EXC-8000PCIe104

Test and Simulation Carrier Board for PCIe/104™ Systems

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

1.1 Overview

The *EXC-8000PCIe104* is a multiprotocol PCIe/104 interface board for avionics test and simulation applications. Each board holds up to four removable modules and one on-board Discrete module. Modules 0–3 can be any of the M8K modules listed in the following table. Module 4 is an on-board Discrete module with 10 channels.

M8K429RT5	ARINC 429 multi-channel interface module. This module supports five ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M8K708	ARINC 708 interface module. This module supports up to two ARINC 708/ 453 channels for the Weather Radar Display Databus. Each channel is selectable as transmit or receive and implements a 64K-word FIFO and supports polling and/or interrupt driven operation.
M8K717-Nx	ARINC 717 interface module. This module supports two ARINC 717 channels; one receive channel and one transmit channel.
M8K825CAN-S5	ARINC 825 interface module. The module supports up to five ARINC 825 channels.
M8KDiscrete	Discrete I/O interface module. This module supports 10 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M8K1553Px	MIL-STD-1553 interface module. The M8K1553Px operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1553PxS	Same as the M8K1553Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1553PxM	Monitor-only version of the M8K1553Px.
M8K1553PxSM	Monitor-only version of the M8K1553PxS.
M8K1760Px	MIL-STD-1760 interface module. The M8K1760Px operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1760PxS	Same as the M8K1760Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1760PxM	Monitor-only version of the M8K1760Px.
M8K1760PxSM	Monitor-only version of the M8K1760PxS.

M8KMMSI-R5	Mini Munitions Store Interface module. This module supports RT, BC/ Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 5 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and a composite monitor output (cBM).
M8KSerial-Jx	Serial communications interface module. This module supports two independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.

All modules come with Windows drivers, including source code.

1.1 Board Features

General Features

- Supported protocols (on up to 4 removable modules):
  - ARINC 429/575 (5 channels per module)
  - ARINC 708/453 (2 channels per module)
  - ARINC 825CAN (5 channels per module)
  - MIL-STD-1553 (single or multifunction)
  - MIL-STD-1760 (single or multifunction)
  - Discrete I/O (10 channels per module)
  - Serial RS485/RS422/RS232 (2 channels per module)
  - MMSI/AS5652 (5 channels per module)
- One on-board Discrete module with 10 Discrete channels
- PCIe/104 stackable up/down bus structure
- Includes a stackthrough PC/104-Plus connector
- 16-bit Count Down Timer
  - 1–65,635 µs resolution
  - Interrupt or global reset upon count down
- Ruggedized and extended temperature options

IRIG B Time Code Input

- Carrier wave:
  - 1KHz Amplitude modulated sine wave
- Rate Designation: 100 peaks per second
- Modulation ratio: 3:1
- Input Amplitude: 0.8–3.5 Vpp (3 Vpp Typ)
- Coded Expressions supported:
  - BCD time-of-year code word
  - Control functions
  - Straight Binary Seconds (SBS) time-of-day
- Application:
  - Synchronization of Time Tags, display and IRIG B time (standard IRIG B120 serial time code)

Physical Characteristics

- Dimensions: 110.2 mm x 95.9 mm
- Weight: 95 g (without removable modules)

Operating Environment

- Temperature: 0°–70°C standard temperature
  -40° to +85°C extended temperature (optional)
- Humidity: 5%–90% noncondensing

Host Interface

- PCI Express compliance: x1 lane PCIe v1.1
- Memory space occupied: 64 MB
- Interrupts: INTA# virtual wire
- Power: Depends on configuration. For more details, see **3.5 Power Requirements** on page 3-12.

Software Support

- *Excalibur Software Tools*: Advanced API with C source code. The Software Tools are available for several operating systems. See the **Downloads** section of our website for a complete list.
- Menu driven software for most of the supported protocols.
- *Exalt Plus*: Excalibur Analysis Laboratory Tools for Windows (optional).

1.1 *EXC-8000PCIe104* Block Diagram

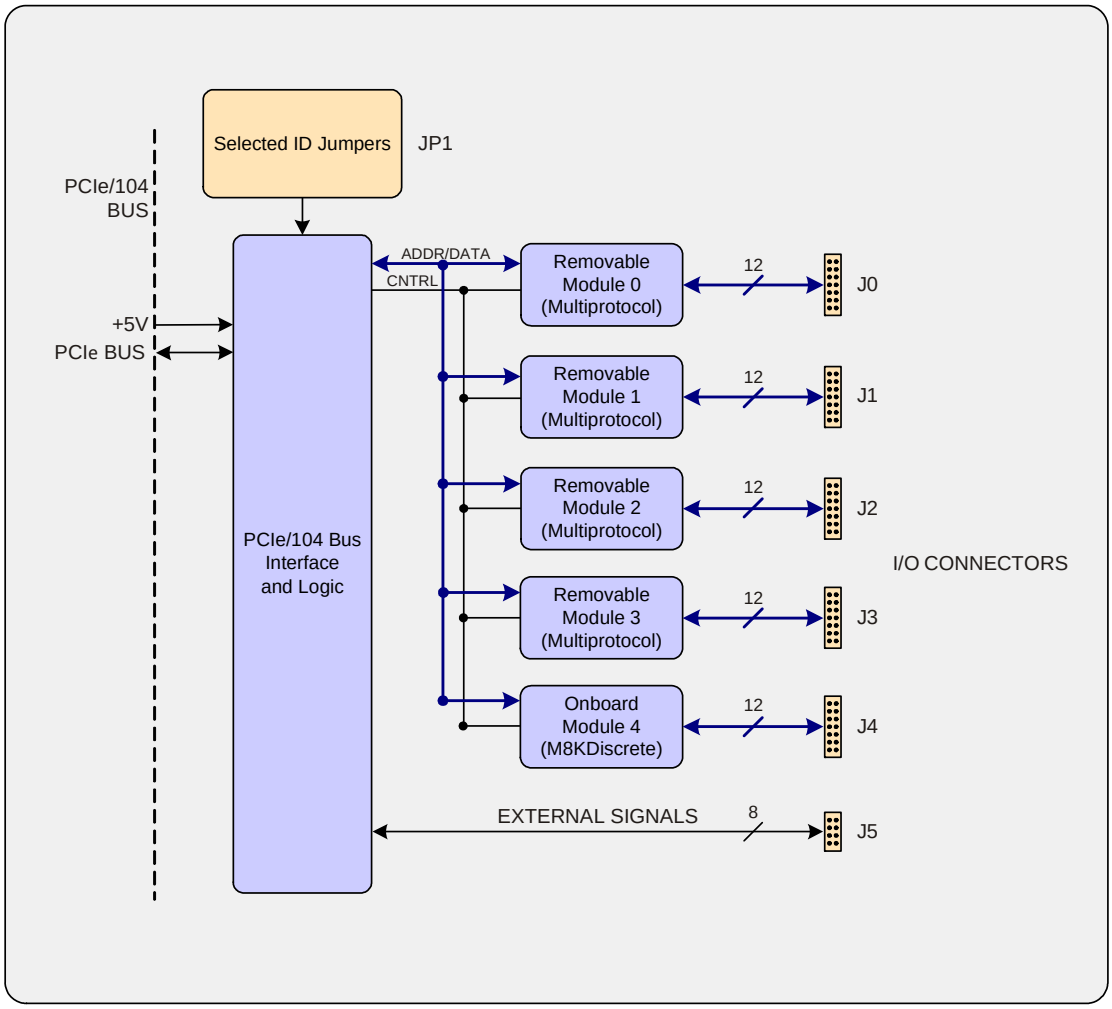

Figure 1-1 *EXC-8000PCIe104* Block Diagram

1.2 Installation

To operate the *EXC-8000PCIe104* board:

1. Install the board in the computer
2. Add Excalibur Software Tools to the hard disk

1.2.1 Installing the Board

Installation of the *EXC-8000PCIe104* board is similar to that of all PCI "Local Bus" boards. The *EXC-8000PCIe104* complies with the "Plug and Play" specification of the PCI standard. As such, its absolute address is determined by the BIOS at start-up.

Warning: Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.

To install the *EXC-8000PCIe104*:

1. Set the Selected ID and PCIe/104 Slot ID Jumpers to the desired configuration. See **Selected ID Jumper [JP1]** on page 3-3.
2. Make certain the computer is OFF. Insert the *EXC-8000PCIe104* into a standard PCIe/104 stack.
3. Attach the adapter cable to the board and to the communication bus. The cable may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

1.2.2 Adding Excalibur Software Tools

The standard software included with the *EXC-8000PCIe104* card is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com

For information about adding the accompanying software drivers, see the **`readme.pdf`** file for the *EXC-8000PCIe104* on the *Excalibur Installation CD*.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the Technical Support page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the Contact Us page of our website. Before contacting Technical Support, please see Information Required for Technical Support.

2 PCI Architecture

Chapter 2 describes the PCI Express architecture. The following topics are covered:

2.1 Memory Structure

The *EXC-8000PCIe104* requests the following memory blocks:

- The first memory block (Base Address Register 0) is 64 MB and contains the memory space for the modules on the board. For more information, see **2.8 Module Memory Space Map** on page 2-18.
- The second memory block (Base Address Register 1) is 32 KB in size and contains the DMA registers. DMA functionality is described in the software tools programmer's reference of each of your board's modules.
- The third memory block (Base Address Register 2) is 8 KB in size and contains the Global registers. For more information, see **2.5 Board Global Registers Map** on page 2-9.

2.2 PCI Configuration Space Header

The board includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The following figure shows the PCI Express Configuration Space Header for PCI Express:

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (Not Used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer – Not Used = 0s				28 H
Base Address Register #5 – Not Used				24 H
Base Address Register #4 – Not Used				20 H
Base Address Register #3 – Reserved				1C H
Base Address Register #2 – Global Registers				18 H
Base Address Register #1 – DMA Registers				14 H
Base Address Register #0 – Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H

Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value: E800 H

Size: 16 bits

The Device Identification register contains the board's device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	Always set to 0
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 1
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the board does not use I/O space, the value of this register is ignored.

Table 2-1 PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information for PCI Express.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	Not used
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 00 (fast timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 0
06	**UDF Supported**	Set to 0
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
03	**Interrupt Status**	This bit is set when an interrupt is received.
00-02	**Reserved**	

Table 2-2 PCI Status Register

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the board.

2.3.6 Class Code Register (CLCD) Address: 09–-0B (H)

Power-up value: FF0000 H

Size: 24 bits

The Class code Register value indicates that the board does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) Address: 0C (H)

Power-up value: 10 H

Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.9 Header Type Register (HDR) Address: 0E (H)

Power-up value: 00 H

Size: 8 bits

The board is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) Address: 0F (H)

Power-up value: 00 H

Size: 8 bits

The Built-In Self-Test register is not implemented in the board.

2.3.11 Base Address Registers (BADR) Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Three memory pages are required by the board: one for the module memory space, one for the Global Registers and one for the DMA registers.

Register	Offset	Size	Function
Base Address 0	10 H	64 MB	Module memory space
Base Address 1	14 H	32 KB	DMA registers
Base Address 2	18 H	8 KB	Global registers

Table 2-3 Base Address Registers Definition

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

The following table describes the bits of the Base Address Register.

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01-02	Always 2 – memory may be mapped anywhere within the 64 bit memory space
00	Always 0 – indicates memory space

Table 2-4 Base Address Register

2.3.12 Cardbus CIS Pointer — Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the board.

2.3.13 Subsystem ID — Address: 2C (H)

Power-up value: 0000 H

Size: 16 bits

2.3.14 Subvendor ID — Address: 2E (H)

Power-up value: 0000 H

Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM) — Address: 30 (H)

Power-up value: 00000000 H

Size: 32 bits

The Expansion ROM Space is not implemented on the board.

2.3.16 PCI Capabilities Pointer

Address: 34 (H)

Power-up value: 50 H

Size: 8 bits

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process.

2.3.17 Interrupt Line Register (INTLN)

Address: 3C (H)

Power-up value: 00 H

Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either "unknown" or "no connection" for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN)

Address: 3D (H)

Power-up value: 01 H

Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT)

Address: 3E (H)

Power-up value: 00 H

Size: 8 bits

The Minimum Grant register is not implemented on the board.

2.3.20 Maximum Latency Register (MAXLAT)

Address: 3F (H)

Power-up value: 00 H

Size: 8 bits

The Maximum Latency register is not implemented on the board.

2.4 Board Global and DMA Registers Memory Space Map

The DMA Registers are mapped as follows.

Figure 2-2 DMA Registers Memory Space Map

The Global Registers are mapped as follows.

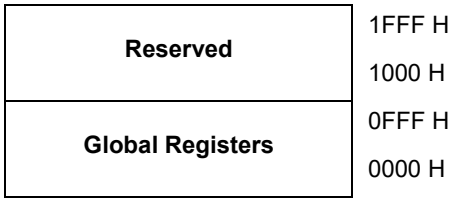

Figure 2-3 Global Registers Memory Space Map

2.5 Board Global Registers Map

The board global registers reside in the second memory block.

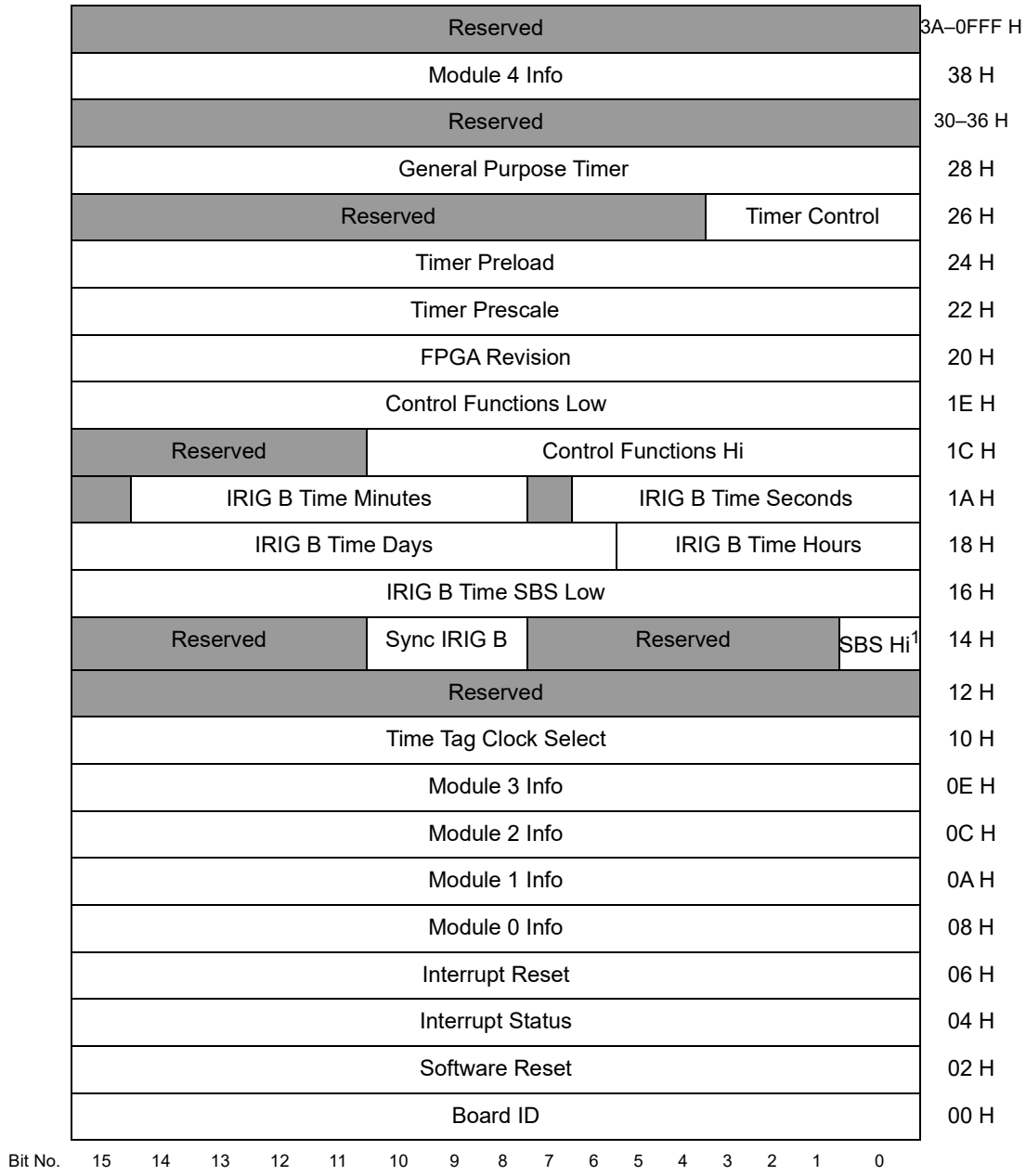

Figure 2-4 Global and IRIG B Registers Map

1. IRIG B Time SBS Hi Register

2.5.1 Board Identification Register

Address: 00 (H)
Length 16 bits

Read only The Board Identification register comprises the following identification items.

Bit	Description
04-15	Hard coded to the value 8E0 H
00-03	Selected ID See **3.3 Selected ID Jumper [JP1]** on page 3-3.

Table 2-5 Board Identification Register

2.5.2 Software Reset Register

Address: 02 (H)
Length 16 bits

Read/Write The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the module's Time Tag counters.

Bit	Description	
06-15	Reserved – set to 0	
05	Module 4 reset	1 = reset module 0 = no effect
04	Global time tag reset	1 = reset all time tag counters 0 = no effect
03	Module 3 reset	1 = reset module 0 = no effect
02	Module 2 reset	1 = reset module 0 = no effect
01	Module 1 reset	1 = reset module 0 = no effect
00	Module 0 reset	1 = reset module 0 = no effect

Table 2-6 Software Reset Register

2.5.3 Interrupt Status Register

Address: 04 (H)
Length 16 bits

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
05-15	Reserved – set to 0
04	1 = indicates that an interrupt was generated by the General Purpose Timer [See **2.7 Global Timer Registers** on page 2-16]
03	1 = indicates that module 3 is interrupting
02	1 = indicates that module 2 is interrupting
01	1 = indicates that module 1 is interrupting
00	1 = indicates that module 0 is interrupting

Table 2-7 Interrupt Status Register

2.5.4 Interrupt Reset Register

Address: 06 (H)
Length 16 bits

Write only The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
05-15	Reserved – set to 0
04	1 = Resets General Purpose Timer interrupt 0 = No effect
03	1 = Resets module 3 interrupt 0 = No effect
02	1 = Resets module 2 interrupt 0 = No effect
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Table 2-8 Interrupt Reset Register

2.5.5 Module Info Registers for Modules 0 – 3

Address: 08, 0A, 0C, 0E (H)
Length 16 bits each

Read only The Module Info Registers provide identification information for each of the modules. (For module 4, see **2.7.5 Module Info Register for Module 4** on page 2-18.)

Bit	Description	
08-15	Module number	00 H = Module 0 Info register 01 H = Module 1 Info register 02 H = Module 2 Info register 03 H = Module 3 Info register
00-07	Module type	24 H = *M8K429RTx* module 25 H = *M8K1553Px* or *M8K1760Px* module 26 H = *M8KMMSI* module 27 H = *M8K708* module 28 H = *M8K825CAN* module 2D H = *M8KDiscrete* module 32 H = *M8KSerial* module 37 H = *M8K717* module 3F H = no module installed

Table 2-9 Module Info Registers

2.5.6 Time Tag Clock Select Register

Address: 10 (H)
Length 16 bits

Read/Write The Time Tag Clock Select Register is used to set either an internal (1 MHz) or external source for the board's Global Time Tag Clock. External Signals are transmitted via connector J5. See **3.4.3 External Signals Connector [J5]** on page 3-10.

Bit	Description	
01-15	Reserved – set to 0	
00	Time Tag Clock Select	1 = External Source 0 = Internal Source [**Default**]

Table 2-10 Time Tag Clock Select Register

2.5.7 FPGA Revision Register

Address: 20 (H)
Length 16 bits

Read only The FPGA Revision register contains the FPGA revision of the board.

2.6 IRIG B Global Registers

The *EXC-8000PCIe104* is able to receive and decode standard serial IRIG B time code format signals via connector J1. The signals are 1 KHz carrier wave, sine wave, amplitude modulated, 100 peaks per second. See **3.4.3 External Signals Connector [J5]** on page 3-10.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the modules on the board.

1st Word	Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.
2nd Word	Set of bits reserved for decoding various control, identification and other special purpose functions.
3rd Word	Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 14 - 1E (H).

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for the location of the registers on the memory map.

Note: The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.

2.6.1 Sync IRIG B Register

Address: 14 (H)
Bits 08 – 10

Read/Write The 3-bit Sync IRIG B register controls the synchronization of a module's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B time registers.

Bit		Description
10	1	Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers
	0	No IRIG B time has been stored in the IRIG B registers. This bit must be reset by the user after the board has written a '1'.
09	1	Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (14-1E [H]) corresponding to the previous valid IRIG B message. If bit 08 is set, then the IRIG B time will be stored at the same time that the Time tags are reset. To calculate the realtime to which the Time tags are synchronized the user will need to **add** '1' to the value of the IRIG B time stored into these registers.
	0	The previous valid IRIG B message should not be stored in the IRIG B registers. This bit will be automatically reset by the board after the storage of the IRIG B time.
08	1	Resets and synchronizes Time Tags of all the modules to the next rising edge of the on-time Reference Point **Pr** of the IRIG B signal. Also sets Bit 09 to a value of '1' in order to store and display the IRIG B time and control functions into the 6 IRIG B registers.
	0	No reset/synchronization of Time tags relative to the **Pr** of the IRIG B signal. This bit will be automatically reset by board after reset of time tags

Table 2-11 Sync IRIGB Register

Note: All bits are read and write.

2.6.2 IRIG B Time SBS High Register

Address: 14 (H)
Bit 0

Read only The IRIG B Time SBS High register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.3 IRIG B Time SBS Low Register

Address: 16 (H)
Bits 15 – 0

Read only The IRIG B Time SBS Low register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.4 IRIG B Time Days Register

Address: 18 (H)
Bits 15 – 6

Read only The IRIG B Time Days register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

2.6.5 IRIG B Time Hours Register

Address: 18 (H)
Bits 5 – 0

Read only The IRIG B Time Hours register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.

2.6.6 IRIG B Time Minutes Register

Address: 1A (H)
Bits 14 – 8

Read only The IRIG B Time Minutes register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.

2.6.7 IRIG B Time Seconds Register

Address: 1A (H)
Bits 6 – 0

Read only The IRIG B Time Seconds register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.

2.6.8 Control Functions Registers

Hi Register Address: 1C (H) / Bits 10 – 0
Low Register Address: 1E (H) / Bits 15 – 0

Read only The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.

2.6.9 FPGA Revision Register

Address: 20 (H)
Bits 15 – 0

Read only The FPGA Revision register contains the FPGA revision of the board.

2.7 Global Timer Registers

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for location of the registers on the memory map.

2.7.1 Timer Prescale Register

Address: 22 (H)
Bits 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Table 2-12 Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.7.2 Timer Preload Register

Address: 24 (H)
Bits 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.7.3 Timer Control Register

Address: 26 (H)
Bits 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose

Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1	Causes global reset of all installed modules
		0	No effect
02	Interrupt on count completed	1	Output an interrupt (see **2.5.3 Interrupt Status Register** on page 2-11)
		0	No effect
01	Reload mode	1	Reload mode
		0	Non-reload/One-shot mode
00	Start/Stop	1	Start
		0	Stop

Table 2-13 Timer Control Register

2.7.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only

The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

2.7.5 Module Info Register for Module 4

Address: 38
Length 16 bits

Read only The Module Info Register provides identification information for Module 4. (For modules 0 – 3, see **2.5.5 Module Info Registers for Modules 0 – 3** on page 2-12.)

Bit	Description	
08-15	Module number	04 H = Module 4 Info register
00-07	Module type	2D H = On-board Discrete module

Table 2-14 Module Info Registers

2.8 Module Memory Space Map

The module memory space map resides in the first memory block. Each module is allocated a space of 128 KB which is mapped as shown in **Figure 2-5 Module Memory Space Map**. (See **Chapter 4 Ordering Information** for information on the available modules for this carrier board.)

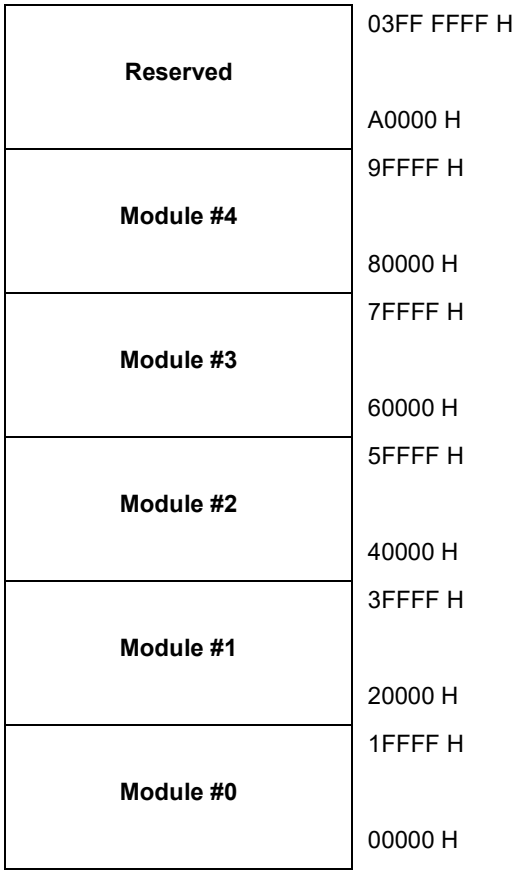

Figure 2-5 Module Memory Space Map

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-8000PCIe104* carrier board.

3.1 *EXC-8000PCIe104* Board Layout

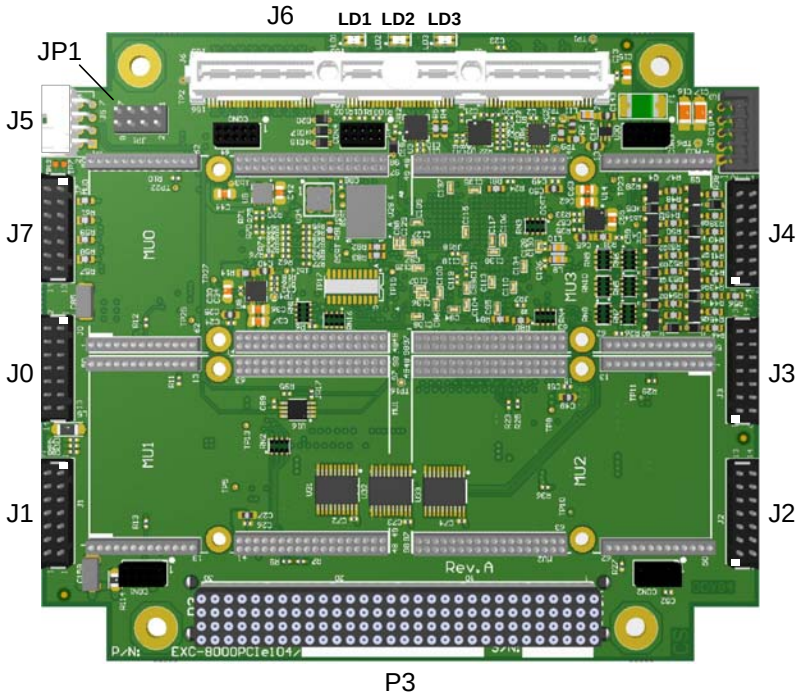

Figure 3-1 ***EXC-8000PCIe104*** **Board Layout – Top View**

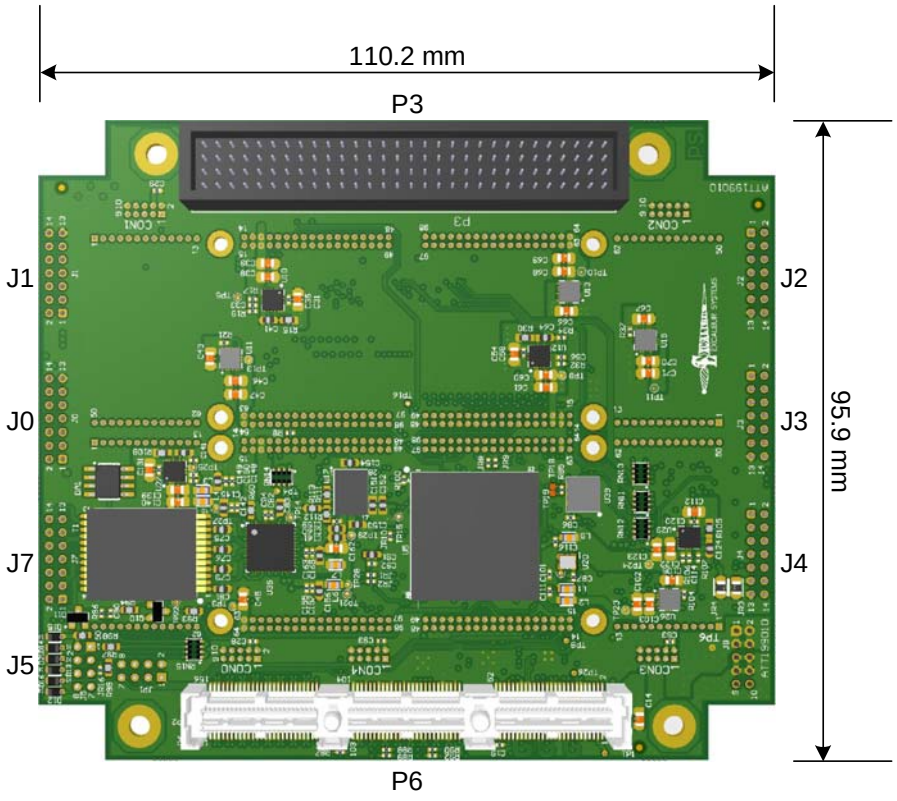

Figure 3-2 ***EXC-8000PCIe104*** **Board Layout – Bottom View**

3.2 Led Indicators

The board contains three dual-color LEDs.

LED	State	Indication
	Red	Module 0 ready
LD1	Green	Module 1 ready
	Red and Green	Modules 0 and 1 ready
	Green	Module 2 ready
LD2	Yellow	Module 3 ready
	Green and Yellow	Module 2 and 3 ready
	Green	Module 4 ready
LD3	Yellow	Hardware ready
	Green and Yellow	Module 4 and hardware ready

Table 3-1 Led Indicators

3.3 Selected ID Jumper [JP1]

The *EXC-8000PCIe104* contains one set of four jumpers [JP1] for the 'Selected ID.' These jumpers can be shorted using 2mm shorting blocks. The Selected ID can be read from the Global Registers. (See section **2.5.1 Board Identification Register** on page 2-10.)

Many *Excalibur Software Tools* functions require the device number as one of its parameters. When using multiple boards, each board's device number must be set using the Excalibur's ExcConfig utility provided with the drivers. When running ExcConfig, you are asked to provide the 'Unique ID' of the board. Use the Selected ID for the Unique ID.

Pins 1, 3 and 5 represent a 3-bit digit of which Pin 5 is the most significant bit. For pin layout, see Figure 3-1.

When a jumper is:

- **Not Installed** – a value of "1" will be set for that bit
- **Installed** – a value of "0" will be set for that bit

Table 3-2 shows the jumper setting for all possible Selected ID numbers.

Selected ID #	Pins 5–6 (Bit 2)	Pins 3–4 (Bit 1)	Pins 2–1 (Bit 0)
0	Installed	Installed	Installed
1	Installed	Installed	Not Installed
2	Installed	Not Installed	Installed
3	Installed	Not Installed	Not Installed
4	Not Installed	Installed	Installed
5	Not Installed	Installed	Not Installed
6	Not Installed	Not Installed	Installed
7	Not Installed	Not Installed	Not Installed

Table 3-2 Selected ID Jumpers

Note: The factory default is Selected ID #7 (no jumpers are installed).

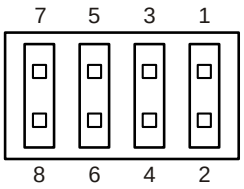

Figure 3-3 JP1 Pin Layout

3.4 Connectors

The *EXC-8000PCIe104* board contains the following connectors:

1. Five 14-pin, 2mm double-row socket header connectors [J0–J4] pass the I/O signals for the modules. Connectors J0–J3 pass the I/O signals for the four removable multiprotocol modules (modules 0–3); and connector J4 passes the I/O signals for the on-board Discrete module (Module 4):
   P/N: Hirose DF11-14DP-2DSA

   A mating connector is provided:
   P/N: Hirose DF11-14DS-2C – Housing
   P/N: Molex® 50394-8200 – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.1 Modules 0–4 Connectors [J0–J4]** on page 3-6.

2. An 8-pin, right angle, dual row, male connector [J5] provides all the external signals:
   P/N: Amphenol FCI 98417-G61-08LF

   A mating crimp housing and crimp terminals are provided:
   P/N: Amphenol FCI 10073599-008LF – Housing
   P/N: Amphenol FCI 77138-101LF – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.3 External Signals Connector [J5]** on page 3-10.

3. A 156-pin, PCIe/104 connector [J6] on top:
   P/N: Samtec ASP-129637-03
4. A 156-pin, PCIe/104 connector [P6] on bottom:
   P/N: Samtec ASP-129646-03

   For a description of the J6 and P6 connector pinouts and signals of these connectors, see section **3.4.2 PCIe/104 Bus I/O Connectors [J6 and P6]** on page 3-8.

5. A 120-pin, elevated socket strip PCI/104 connector [P3], centerline 2mm, passes all of the PCI I/O signals:
   P/N: Samtec ESQT-130-02-G-Q-368

   A plastic shroud is provided to protect the exposed pins on bottom:
   P/N: Samtec ATS-30-Q

   The connector is used for stack-through purposes and has no signals connected to the board.

3.4.1 Modules 0–4 Connectors [J0–J4]

Five 14-pin, 2mm double-row socket header connectors [J0–J4] pass the I/O signals for the modules. Connectors J0–J3 pass the I/O signals for the four multiprotocol modules (modules 0–3); and connector J4 passes the I/O signals for the on-board Discrete module (Module 4). For connector part numbers, see **3.4 Connectors** on page 3-5.

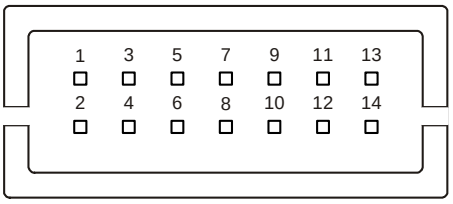

Figure 3-4 Modules 0–4 Connector Layout [J0–J4] – Top View

Pin #	Module Signals										
	M8K429RT5	**M8K717**	**M8K825CAN**	**M8K1553Px[M] M8K1553PxSM M8K1760Px[M] M8K1760PxSM**	**M8K1553PxS M8K1760PxS**	**M8K708**	**M8KDiscrete (Including the on-board module)**	**M8KSerial RS-232**	**M8KSerial RS-422**	**M8KSerial RS-485**	**M8KMMSI**
1	Channel 0 Low	N/C	Channel 0 Low	Bus A Low	Bus A Low	Channel 0 Low	I/O Channel 0	Reserved	Channel 0 Transmit High	Channel 0 High	Channel 0 Low
3	Channel 0 High	N/C	Channel 0 High	Bus A High	Bus A High	Channel 0 High	I/O Channel 1	Channel 0 Transmit	Channel 0 Transmit Low	Channel 0 Low	Channel 0 High
5	Channel 1 Low	N/C	Channel 1 Low	Reserved	RT address bit position 0 input[1]	Reserved	I/O Channel 2	Channel 0 Receive	Channel 0 Receive High	Reserved	Channel 1 Low
7	Channel 1 High	N/C	Channel 1 High	Reserved	RT address bit position 1 input[1]	Reserved	I/O Channel 3	Reserved	Channel 0 Receive Low	Reserved	Channel 1 High
13	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
9	Channel 2 Low	N/C	Channel 2 Low	Reserved	RT address bit position 2 input[1]	Reserved	I/O Channel 4	Ground	Ground	Ground	Channel 2 Low
11	Channel 2 High	N/C	Channel 2 High	Reserved	RT address bit position 3 input[1]	Reserved	Ground for Channels 0–4	Shield	Shield	Shield	Channel 2 High
2	Channel 3 Low	N/C	Channel 3 Low	Reserved	RT address bit position 4 input[1]	Reserved	I/O Channel 5	Reserved	Channel 1 Transmit High	Channel 1 High	Channel 3 Low
4	Channel 3 High	N/C	Channel 3 High	Reserved	RT address parity bit[2]	Reserved	I/O Channel 6	Channel 1 Transmit	Channel 1 Transmit Low	Channel 1 Low	Channel 3 High
6	Channel 4 Low	Transmit Channel Low	Channel 4 Low	Bus B Low	Bus B Low	Channel 1 Low	I/O Channel 7	Channel 1 Receive	Channel 1 Receive High	Reserved	Channel 4 Low
8	Channel 4 High	Transmit Channel High	Channel 4 High	Bus B High	Bus B High	Channel 1 High	I/O Channel 8	Reserved	Channel 1 Receive Low	Reserved	Channel 4 High
10	Channel 5 Low	Receive Channel Low	Channel 5 Low	Reserved	RT address lock bit[3]	Reserved	I/O Channel 9	Ground	Ground	Ground	Channel 5 Low
12	Channel 5 High	Receive Channel High	Channel 5 High	Ground	Ground	Ground	Ground for Channels 5–9	Shield	Shield	Shield	Channel 5 High
14	Shield	Shield	Shield	Shield	Shield	Shield	Shield	Shield	Shield	Shield	Shield

Table 3-3 J0–J4 Connector Pinouts

1. Pin shorted to ground = logic 0
   Open = logic 1
   See **RT Number Register** in the *M8K1553Px Module User's Manual.*
2. This bit is appended to the remote terminal address bus to supply parity. Odd parity is required for proper operation.
3. 0 = RT number locked (RT address is set to the value represented by pins 5, 7, 9, 11, 2, 4.
   1 = RT number unlocked (RT address can be changed by writing to the module's RT Number Register).

3.4.2 PCIe/104 Bus I/O Connectors [J6 and P6]

Standard PCIe/104 connectors, [J6] on top and [P6] on the bottom, pass all the relevant PCIe signals to the *EXC-8000PCIe104*. For connector part numbers, see **3.4 Connectors** on page 3-5.

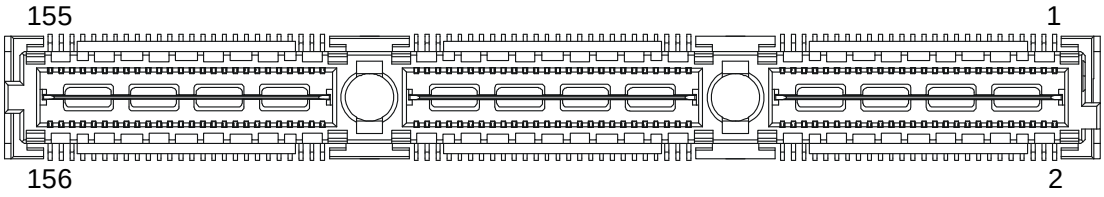

Figure 3-5 PCIe/104 Bus I/O Connector on Top of Board [J6] – Top View

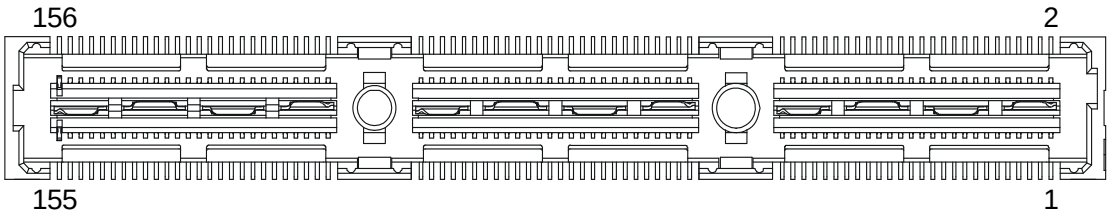

Figure 3-6 PCIe/104 Bus I/O Connector on Bottom of Board [P6] – Top View

J6 Pin #	Signal Name		J6 Pin #	Signal Name
1	USB_OC#		2	PE_RST#
3	3.3V		4	3.3V
5	USB_1p		6	USB_0p
7	USB_1n		8	USB_0n
9	GND		10	GND
11	PEx1_1Tp		12	PEx1_0Tp
13	PEx1_1Tn		14	PEx1_0Tn
15	GND		16	GND
17	PEx1_2Tp		18	PEx1_3Tp
19	PEx1_2Tn		20	PEx1_3Tn
21	GND		22	GND
23	PEx1_1Rp		24	PEx1_0Rp
25	PEx1_1Rn	+5V	26	PEx1_0Rn
27	GND		28	GND
29	PEx1_2Rp		30	PEx1_3Rp
31	PEx1_2Rn		32	PEx1_3Rn
33	GND		34	GND
35	PEx1_1Clkp		36	PEx1_0Clkp
37	PEx1_1Clkn		38	PEx1_0Clkn
39	5V_Always		40	5V_Always
41	PEx1_2Clkp		42	PEx1_3Clkp
43	PEx1_2Clkn		44	PEx1_3Clkn
45	CPU_DIR		46	PWRGOOD
47	SMB_DAT		48	PEx16_x8_x4_Clkp
49	SMB_CLK		50	PEx16_x8_x4_Clkn
51	SMB_ALERT		52	PSON#
53	Reserved/WAKE#		54	PEG_ENA#
55	GND		56	GND
57	PEx16_0T(8)p		58	PEx16_0T(0)p
59	PEx16_0T(8)n		60	PEx16_0T(0)n
61	GND		62	GND
63	PEx16_0T(9)p		64	PEx16_0T(1)p
65	PEx16_0T(9)n		66	PEx16_0T(1)n
67	GND		68	GND
69	PEx16_0T(10)p		70	PEx16_0T(2)p
71	PEx16_0T(10)n		72	PEx16_0T(2)n
73	GND		74	GND
75	PEx16_0T(11)p		76	PEx16_0T(3)p
77	PEx16_0T(11)n	+5V	78	PEx16_0T(3)n
79	GND		80	GND
81	PEx16_0T(12)p		82	PEx16_0T(4)p
83	PEx16_0T(12)n		84	PEx16_0T(4)n
85	GND		86	GND
87	PEx16_0T(13)p		88	PEx16_0T(5)p
89	PEx16_0T(13)n		90	PEx16_0T(5)n
91	GND		92	GND
93	PEx16_0T(14)p		94	PEx16_0T(6)p
95	PEx16_0T(14)n		96	PEx16_0T(6)n
97	GND		98	GND
99	PEx16_0T(15)p		100	PEx16_0T(7)p
101	PEx16_0T(15)n		102	PEx16_0T(7)n
103	GND		104	GND
105	SDVO_DAT(PENA#)		106	SDVO_CLK
107	GND		108	GND
109	PEx16_0R(8)p		110	PEx16_0R(0)p
111	PEx16_0R(8)n		112	PEx16_0R(0)n
113	GND		114	GND
115	PEx16_0R(9)p		116	PEx16_0R(1)p
117	PEx16_0R(9)n		118	PEx16_0R(1)n
119	GND		120	GND
121	PEx16_0R(10)p		122	PEx16_0R(2)p
123	PEx16_0R(10)n		124	PEx16_0R(2)n
125	GND		126	GND
127	PEx16_0R(11)p		128	PEx16_0R(3)p
129	PEx16_0R(11)n	+12V	130	PEx16_0R(3)n
131	GND		132	GND
133	PEx16_0R(12)p		134	PEx16_0R(4)p
135	PEx16_0R(12)n		136	PEx16_0R(4)n
137	GND		138	GND
139	PEx16_0R(13)p		140	PEx16_0R(5)p
141	PEx16_0R(13)n		142	PEx16_0R(5)n
143	GND		144	GND
145	PEx16_0R(14)p		146	PEx16_0R(6)p
147	PEx16_0R(14)n		148	PEx16_0R(6)n
149	GND		150	GND
151	PEx16_0R(15)p		152	PEx16_0R(7)p
153	PEx16_0R(15)n		154	PEx16_0R(7)n
155	GND		156	GND

P6 Pin #	Signal Name		P6 Pin #	Signal Name
2	PE_RST#		1	USB_OC#
4	3.3V		3	3.3V
6	USB_0p		5	USB_1p
8	USB_0n		7	USB_1n
10	GND		9	GND
12	PEx1_0Tp		11	PEx1_1Tp
14	PEx1_0Tn		13	PEx1_1Tn
16	GND		15	GND
18	PEx1_3Tp		17	PEx1_2Tp
20	PEx1_3Tn		19	PEx1_2Tn
22	GND		21	GND
24	PEx1_0Rp		23	PEx1_1Rp
26	PEx1_0Rn	+5V	25	PEx1_1Rn
28	GND		27	GND
30	PEx1_3Rp		29	PEx1_2Rp
32	PEx1_3Rn		31	PEx1_2Rn
34	GND		33	GND
36	PEx1_0Clkp		35	PEx1_1Clkp
38	PEx1_0Clkn		37	PEx1_1Clkn
40	5V_Always		39	5V_Always
42	PEx1_3Clkp		41	PEx1_2Clkp
44	PEx1_3Clkn		43	PEx1_2Clkn
46	PWRGOOD		45	CPU_DIR
48	PEx16_x8_x4_Clkp		47	SMB_DAT
50	PEx16_x8_x4_Clkn		49	SMB_CLK
52	PSON#		51	SMB_ALERT
54	PEG_ENA#		53	Reserved/WAKE#
56	GND		55	GND
58	PEx16_0T(0)p		57	PEx16_0T(8)p
60	PEx16_0T(0)n		59	PEx16_0T(8)n
62	GND		61	GND
64	PEx16_0T(1)p		63	PEx16_0T(9)p
66	PEx16_0T(1)n		65	PEx16_0T(9)n
68	GND		67	GND
70	PEx16_0T(2)p		69	PEx16_0T(10)p
72	PEx16_0T(2)n		71	PEx16_0T(10)n
74	GND		73	GND
76	PEx16_0T(3)p		75	PEx16_0T(11)p
78	PEx16_0T(3)n	+5V	77	PEx16_0T(11)n
80	GND		79	GND
82	PEx16_0T(4)p		81	PEx16_0T(12)p
84	PEx16_0T(4)n		83	PEx16_0T(12)n
86	GND		85	GND
88	PEx16_0T(5)p		87	PEx16_0T(13)p
90	PEx16_0T(5)n		89	PEx16_0T(13)n
92	GND		91	GND
94	PEx16_0T(6)p		93	PEx16_0T(14)p
96	PEx16_0T(6)n		95	PEx16_0T(14)n
98	GND		97	GND
100	PEx16_0T(7)p		99	PEx16_0T(15)p
102	PEx16_0T(7)n		101	PEx16_0T(15)n
104	GND		103	GND
106	SDVO_CLK		105	SDVO_DAT(PENA#)
108	GND		107	GND
110	PEx16_0R(0)p		109	PEx16_0R(8)p
112	PEx16_0R(0)n		111	PEx16_0R(8)n
114	GND		113	GND
116	PEx16_0R(1)p		115	PEx16_0R(9)p
118	PEx16_0R(1)n		117	PEx16_0R(9)n
120	GND		119	GND
122	PEx16_0R(2)p		121	PEx16_0R(10)p
124	PEx16_0R(2)n		123	PEx16_0R(10)n
126	GND		125	GND
128	PEx16_0R(3)p		127	PEx16_0R(11)p
130	PEx16_0R(3)n	+12V	129	PEx16_0R(11)n
132	GND		131	GND
134	PEx16_0R(4)p		133	PEx16_0R(12)p
136	PEx16_0R(4)n		135	PEx16_0R(12)n
138	GND		137	GND
140	PEx16_0R(5)p		139	PEx16_0R(13)p
142	PEx16_0R(5)n		141	PEx16_0R(13)n
144	GND		143	GND
146	PEx16_0R(6)p		145	PEx16_0R(14)p
148	PEx16_0R(6)n		147	PEx16_0R(14)n
150	GND		149	GND
152	PEx16_0R(7)p		151	PEx16_0R(15)p
154	PEx16_0R(7)n		153	PEx16_0R(15)n
156	GND		155	GND

Table 3-4 PCIe/104 Bus I/O Connectors J6 and P6 Pinouts

3.4.3 External Signals Connector [J5]

An 8-pin, right angle, dual row, male connector [J5] provides all the external signals. For connector part numbers, see **3.4 Connectors** on page 3-5.

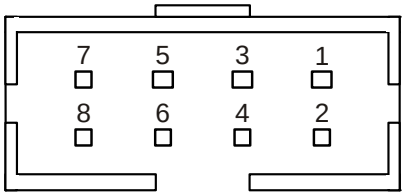

Figure 3-7 External Signals Connector Layout [J5] – Front View

J7 Pin #	Signal Name	J7 Pin #	Signal Name
1	EXTTCLKI	**2**	EXTTRSTn
3	EXTTCLKO	**4**	GND
5	RESERVED	**6**	IRIG B
7	SHIELD	**8**	EXTTRSOn

Figure 3-8 External Signals Connector Pinouts [J5]

Signal	Description
EXTTCLKI	**External Time Tag Clock Input** (Nominal value: 1MHz). This signal supplies an external global clock for the Time Tags of all the modules. Use the signal to synchronize the Time Tags that are implemented on the modules[1] to other boards or systems.[2] See Time Tag Clock Select Register, page 2-12.
EXTTCLKO	**Global Time Tag Clock TTL Output** (1 MHz). This signal is the Global Clock that is supplied to all the modules for their Time Tags. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules.[1] The source of this clock is either the External Time Tag Clock **EXTTCLKI**[2] or the Internal Time Tag Clock. See Time Tag Clock Select Register, page 2-12
EXTTRSTn	**External Time Tag reset TTL Input** Use this low active pulsed signal (minimum 100 nsec.wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems.[2]
EXTTRSOn	**Global Time Tag Reset TTL Output** This low active signal is activated each time a Global Time Tag Reset is applied. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules.[1] This signal is activated by either the internal Global Time Tag signal See Software Reset Register, page 2-10 or from the External Time Tag signal (**EXTTRSOn**).[2]
IRIG B	**IRIG B Input** This should be a 1KHz sine wave, amplitude modulated, IRIG B signal with a 3:1 modulation ratio at 3V typical.
GND	Provides ground reference for the digital signal connections.
SHIELD	Provided for a cables shield connection. This signal is connected to the case of the computer through the mechanical holes.

Table 3-5 External Signal Connector Signal Descriptions [J5]

1. See the manual for each module for a description of how the Time Tag clock is implemented, if used, for that module.
2. See **3.4.3.1 Synchronizing with an External Source** and **3.4.3.2 Synchronize Between Excalibur Boards** on page 3-11.

3.4.3.1 Synchronizing with an External Source

To synchronize an external system to a single *EXC-8000PCIe104* board, the EXTTCLKO and the EXTTRSOn signals need to be connected to the external clock source and the external reset respectively.

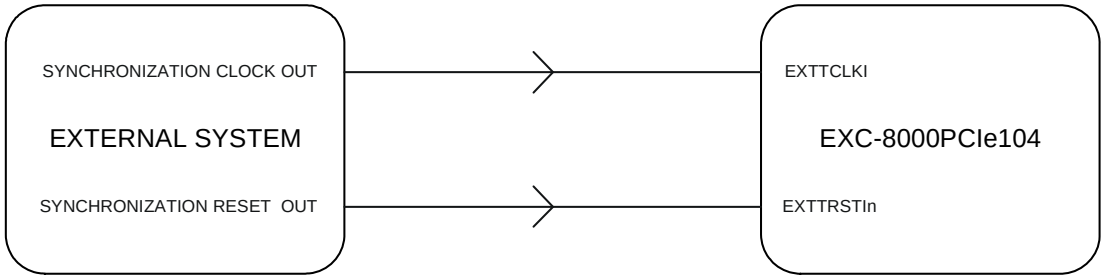

Figure 3-9 Synchronization of an External System to a Single *EXC-8000PCIe104* Board

Warning: The synchronization clock and reset signals may be connected to multiple targets to achieve system wide synchronization.

3.4.3.2 Synchronize Between Excalibur Boards

To synchronize multiple Excalibur boards the **EXTCLKO** and the **EXTTRSOn** signals of one board need to be connected to all the **ETTCLKI** and the **EXTTRSTn** signals respectively, of the remaining boards.

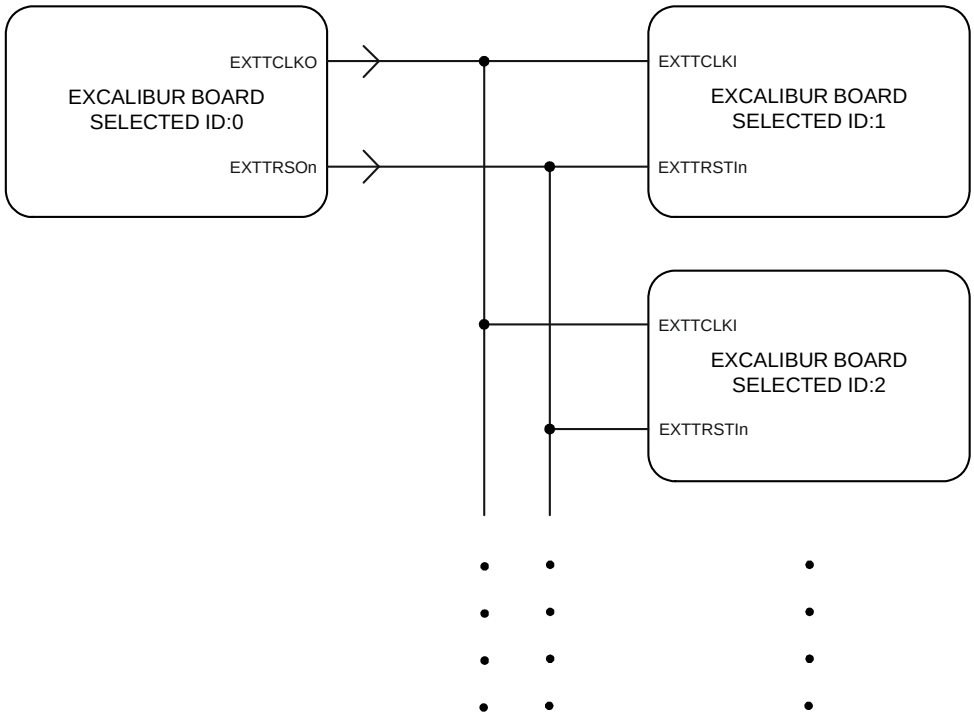

Figure 3-10 Synchronization Between Excalibur Boards

3.5 Power Requirements

The recommended power requirements for the *EXC-8000PCIe104* are:

- 430 mA @ +5 V for the base board only, including the on-board Discrete module.
- For each installed module, add the power requirements listed in the *User's Manual* for that module.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering.

Basic Part #	Option	Description
EXC-8000PCIe104/*xx*		Multiprotocol carrier board for PCIe/104 compatible systems, with up to four removable modules and one on-board Discrete module.
	-E	Add this suffix for the extended temperature option (-40° to +85°C).
	-R	Add this suffix for ruggedized option (bonded components)
	-001	Add this suffix for conformal coating.

Table 4-1 Ordering Information

Table 4-2 lists the **module codes** to use when ordering the carrier board and modules. Replace "***xx***" in the above ordering code with the **module codes** of the modules you want, for up to four modules. (Use the **module part #** when ordering a module separate from a carrier board.) See the notes after Table 4-2 for ordering examples.

Currently the following module options are available:

Protocol Type	Module Part #	Module Code	Description
ARINC 429	**M8K429RT5**	**A0**	ARINC 429 module with 5 channels, software selectable as transmit or receive.
ARINC 708/453	**M8K708**	**C0**	ARINC 708/453 with 2 channels, software selectable as transmit or receive.
ARINC 717	**M8K717-Nx**	**Nx**	ARINC 717 module with 2 channels, one transmit and one receive. Replace '**N*x***' with one of the following: **N1** = HBP transmit channel **N2** = BPRZ transmit channel
ARINC 825	**M8K825CAN-S5**	**S5**	ARINC 825 module with 5 channels.
MIL-STD-1553	**M8K1553Px**	**F0**	MIL-STD-1553 multi-function module, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1553 Single Function	**M8K1553PxS-Tx**	**Tx**	MIL-STD-1553 single function module. Replace '**T*x***' with one of the following: **T1** = Transformer coupled mode **T2** = Direct coupled mode
MIL-STD-1553 Monitor Only	**M8K1553PxM**	**G0**	MIL-STD-1553 module for monitoring only (transmit disabled).

Table 4-2 Protocol Codes

Protocol Type	Module Part #	Module Code	Description
MIL-STD-1553 Single Function Monitor Only	**M8K1553PxSM-Vx**	**Vx**	MIL-STD-1760 single function module for monitoring only (transmit disabled). Replace '**V*x***' with one of the following: **V1** = Transformer coupled mode **V2** = Direct coupled mode
MIL-STD-1760	**M8K1760Px**	**L0**	MIL-STD-1760 multi-function module, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1760 Single Function	**M8K1760PxS-Hx**	**Hx**	MIL-STD-1760 single function module. Replace '**H*x***' with one of the following: **H1** = Transformer coupled mode **H2** = Direct coupled mode
MIL-STD-1760 Monitor Only	**M8K1760PxM**	**M0**	MIL-STD-1760 module for monitoring only (transmit disabled).
MIL-STD-1760 Single Function Monitor Only	**M8K1760PxSM-Kx**	**Kx**	MIL-STD-1760 single function module for monitoring only (transmit disabled). Replace '**K*x***' with one of the following: **K1** = Transformer coupled mode **K2** = Direct coupled mode
MMSI	**M8KMMSI-R5**	**R5**	MMSI module with 5 EBR hub ports and 1 cBM port.
Discrete	**M8KDiscrete**	**I0**	Discrete module with 10 channels, software selectable as input/output and TTL/Avionics 0–32V thresholds.
Serial	**M8KSerial-J*x***	**J*x***	Serial module with 2 channels, software selectable for RS-232 up to 3 Mbps and RS-422 and RS-485 up to 4 Mbps. Replace '**J*x***' with one of the following: **J1** = Channel 0 is RS-232; Channel 1 is RS-232 **J2** = Channel 0 is RS-232; Channel 1 is RS-485 **J3** = Channel 0 is RS-232; Channel 1 is RS-422 **J4** = Channel 0 is RS-485; Channel 1 is RS-485 **J5** = Channel 0 is RS-485; Channel 1 is RS-422 **J6** = Channel 0 is RS-422; Channel 1 is RS-422

Table 4-2 Protocol Codes (Continued)

Note:

- When ordering a board with a number of different protocol modules, the module codes must be in the following form:

  Example: EXC-8000PCIe104/A0B1C0D0

  The first module code in the part number is Module 0, the second is Module 1, and so on.

- If one or more empty module locations are required in between other modules, insert an asterisk (*).

Example: EXC-8000PCIe104/A0*F0

This is an *EXC-8000PCIe104* board with:

1 *M8K429RT5* module at module location 0.
Module location 1 is empty.
1 *M8K1553Px* module at module location 2.
Module location 3 is empty
1 onboard *M8KDiscrete* module at module location 4.

Example: EXC-8000PCIe104/J2J3

This is an *EXC-8000PCIe104* board with:

M8KSerial module with channel 0 as RS-232 and channel 1 as RS-485 at module location 0.
M8KSerial module with channel 0 as RS-232 and channel 1 as RS-422 at module location 1.
Module locations 2 and 3 are empty
1 onboard *M8KDiscrete* module at module location 4.

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