EXC-4000P104plus

Test and Simulation Carrier Board for PC/104-*Plus* Systems

User's Manual

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1 Introduction

1.1 Overview

The *EXC-4000P104plus* is a multiprotocol PC/104-*Plus* interface board for avionics test and simulation applications. Each board holds up to five independent modules.

- Module 0 is an M4K429RTx built-in module.
- Module 1 can be any of the M4K modules listed in the following table.
- Module 2 can be any of the M4K modules listed in the following table.
- Module 3 is an M4K1553P*x* built-in module.
- Module 4 is an M4K1553P*x* built-in module.

M4K1553P*x*	MIL-STD-1553 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. Supports an Internal Concurrent Monitor in RT and BC/RT modes.
M4K1553P*x*-1760	Same as M4K1553Px plus MIL-STD-1760 options.
M4K1553MCH	MIL-STD-1553 single function interface module. This module is qualified for airborne applications. (Not available for PCI Express-based carrier boards.)
M4K429RT*x*	ARINC 429 multi-channel interface module. This module supports either five or ten ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M4KDiscrete	Discrete I/O interface module. This module supports 20 bi-directional discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M4KSerial	Serial communications interface module. This module supports either two or four independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.
M4KCAN	CAN protocol interface module. This module supports either two, four or six independent channels of CAN 2.0B protocol with standard and extended message frames and message identifiers.
M4K708	ARINC 708 interface module. This module supports two channels of ARINC 708/453, each one selectable as either transmit or receive
M4KMMSI	Mini Munitions Store Interface module. This module supports RT, BC/ Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 8 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and 1 monitor output.
M4KH009	H009 interface module. This double size module supports a fully functional H009 channel (CCC, multi-PU,MON) and a concurrent Bus Monitor.

All modules come with Windows drivers, including source code and mating connectors.

Excalibur also offers a single module ARINC 429 version of the *EXC-4000P104plus* board. This board has only one module, at module location 0. This board does not have the option of adding any additional modules.

For ordering information, see **Chapter 4 Ordering Information.**

EXC-4000P104plus Board Features

General Specifications	
EXC-4000P104plus	A standard PC/104-*Plus* board with a stackthrough PC/104 connector
Supports up to five modules	
Protocols supported:	ARINC 429/575 (5 or 10 channels per module) ARINC 708/453 MIL-STD-1553 (Px, MCH and compatible) MIL-STD-1760 Discrete I/O Serial - RS485/RS422/RS232 CAN MMSI H009
Timer	16-bit count down timer
Resolution	1 μs min, 65536 μs max
Output	Interrupt, Global reset
Operating Environment	
Temperature:	0° - 70°C standard temp. -40° to +85°C extended temp. (optional)
Humidity:	5% – 90% non-condensing
Physical Characteristics	
Dimension	110.5mm – 95.88mm
Weight	100g (without modules 1 and 2)
Host Interface	
PCI compliance:	Universal target 8/16 bit
Memory space occupied:	512 Kbytes (128K per module)
Interrupts:	INTA#
Power	Depends on configuration
IRIG B Time Code Input	
Carrier wave	1KHz Amplitude modulated sine wave
Rate Designation	100 peaks per second
Modulation ratio	3:1
Input Amplitude	0.8 Vpp min, 3.5 Vpp max, 3 Vpp Typ
Coded Expressions supported	BCD Time-of-Year code word, Control functions, straight binary seconds time-of-day (seconds-of-day)
Application	Synchronization of Time Tags, display and IRIG B time

Software Support

C Drivers with source code
Mystic Windows software for ARINC 429 modules
MerlinPlus Windows software for Px modules
Merlin Windows software for MCH modules
Exalt Plus (Optional - contact your Excalibur representative for details)

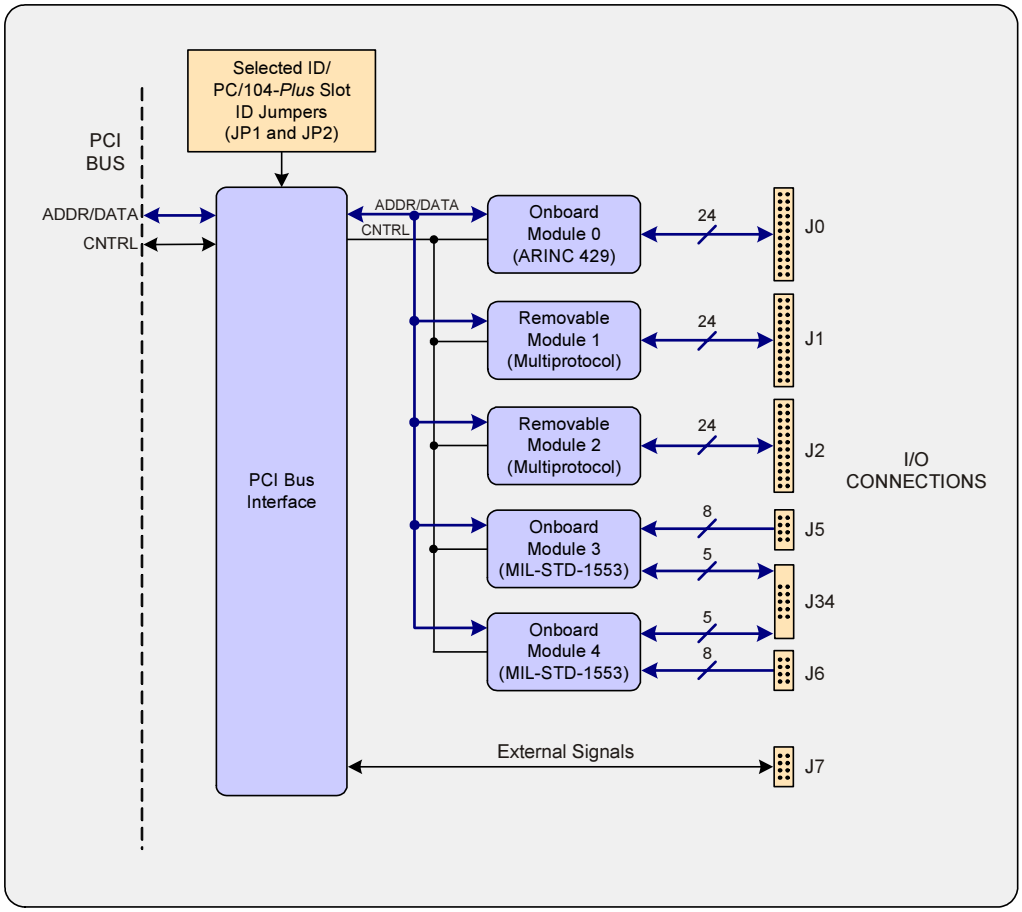

Figure 1-1 *EXC-4000P104plus* Block Diagram

Note: J5/J6 are only used when Module 3 and/or Module 4 are single function *M4K1553PxS* modules.

1.2 Installation

To operate the *EXC-4000P104plus* board:

1. Install the board in the computer
2. Add Excalibur Software Tools to the hard disk

1.2.1 Installing the Board

Installation of the *EXC-4000P104plus* board is similar to that of all PCI "Local Bus" boards. The *EXC-4000P104plus* complies with the "Plug and Play" specification of the PCI standard. As such, its absolute address is determined by the BIOS at start-up.

Warning: Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.

To install the *EXC-4000P104plus*:

1. Set the **Selected ID and** PC/104-*Plus* **Slot ID Jumpers** to the desired configuration. See **Jumpers** on page 3-3.
2. Make certain the computer is OFF. Insert the *EXC-4000P104plus* into a standard PC/104-*Plus* computer.
3. Attach the adapter cable to the board and to the communication bus. The cable may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

1.2.2 Adding Excalibur Software Tools

The standard software included with the *EXC-4000P104plus* card is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com

For information about adding the accompanying software drivers, see the **`readme.pdf`** file for the *EXC-4000P104plus* on the *Excalibur Installation CD*.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:

2.1 Memory Structure

The *EXC-4000P104plus* requests two memory blocks:

The first memory block is 1MB in size and contains the memory space for the modules on the carrier board.

The second memory block is 128 bytes in size and contains the Global Registers which are explained in more detail in section **2.5 EXC-4000P104plus Global Registers Map** on page 2-9.

2.2 PCI Configuration Space Header

The *EXC-4000P104plus* includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (not used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer (not used = 0s)				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2 (not used)				18 H
Base Address Register #1 – Global Registers				14 H
Base Address Register #0 Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H

Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value: 4007 H

Size: 16 bits

The Device Identification register contains the *EXC-4000P104plus* device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	Always set to 1
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 0
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the *EXC-4000P104plus* board does not use I/O space, the value of this register is ignored.

PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	Not used
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 10 (slow timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 1
06	**Reserved**	
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
00-03	**Reserved**	

PCI Status Register

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the *EXC-4000P104plus*.

2.3.6 Class Code Register (CLCD) Address: 09–0B (H)

Power-up value: FF0000 H

Size: 24 bits

The Class code Register value indicates that the *EXC-4000P104plus* does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) Address: 0C (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.9 Header Type Register (HDR) Address: 0E (H)

Power-up value: 00 H

Size: 8 bits

The *EXC-4000P104plus* is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) Address: 0F (H)

Power-up value: 00 H

Size: 8 bits

The Built-In Self-Test register is not implemented in the *EXC-4000P104plus*.

2.3.11 Base Address Registers (BADR)

Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Two memory pages are required by the *EXC-4000P104plus:* one for the module memory space and one for the Global Registers.

Register	Offset	Size	Function
Base Address 0	10 H	1MB	Module memory space
Base Address 1	14 H	128 Bytes	Global registers

Base Address Registers Definition

Each Base Address Register contains 32 bits:

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 0 – memory is not prefetchable
01-02	Always 0 – memory may be mapped anywhere
00	Always 0 – indicates memory space

Base Address Register

2.3.12 Cardbus CIS Pointer

Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the *EXC-4000P104plus*.

2.3.13 Subsystem ID — Address: 2C (H)

Power-up value: 0000 H
Size: 16 bits

2.3.14 Subvendor ID — Address: 2E (H)

Power-up value: 0000 H
Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM) — Address: 30 (H)

Power-up value: 00000000 H
Size: 32 bits

The Expansion ROM Space is not implemented on the *EXC-4000P104plus*.

2.3.16 Reserved — Address: 34–3A (H)

Power-up value: 0000000000000000 H
Size: 64 bits

2.3.17 Interrupt Line Register (INTLN) — Address: 3C (H)

Power-up value: 00 H
Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either "unknown" or "no connection" for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) — Address: 3D (H)

Power-up value: 01 H
Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) Address: 3E (H)

Power-up value: 00 H

Size: 8 bits

The Minimum Grant register is not implemented on the *EXC-4000P104plus*.

2.3.20 Maximum Latency Register (MAXLAT) Address: 3F (H)

Power-up value: 00 H

Size: 8 bits

The Maximum Latency register is not implemented on the *EXC-4000P104plus*.

2.4 EXC-4000P104plus Module Memory Space Map

The module memory space map resides in the first memory block. Each module is allocated a space of 128KB which is mapped as shown in **Figure 2-2 Module Memory Space Map.**

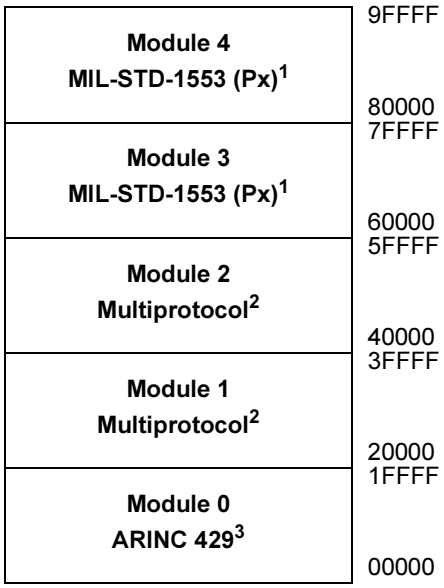

Figure 2-2 Module Memory Space Map

1. See the *M4K1553Px User's Guide* for a detailed description of the operation of this module.
2. See the *User's Manual* for the specific module installed for a detailed description of the operation of this module.
3. See the *M4K429RTx User's Manual* for a detailed description of the operation of this module.

2.5 EXC-4000P104plus Global Registers Map

The board global registers reside in the second memory block.

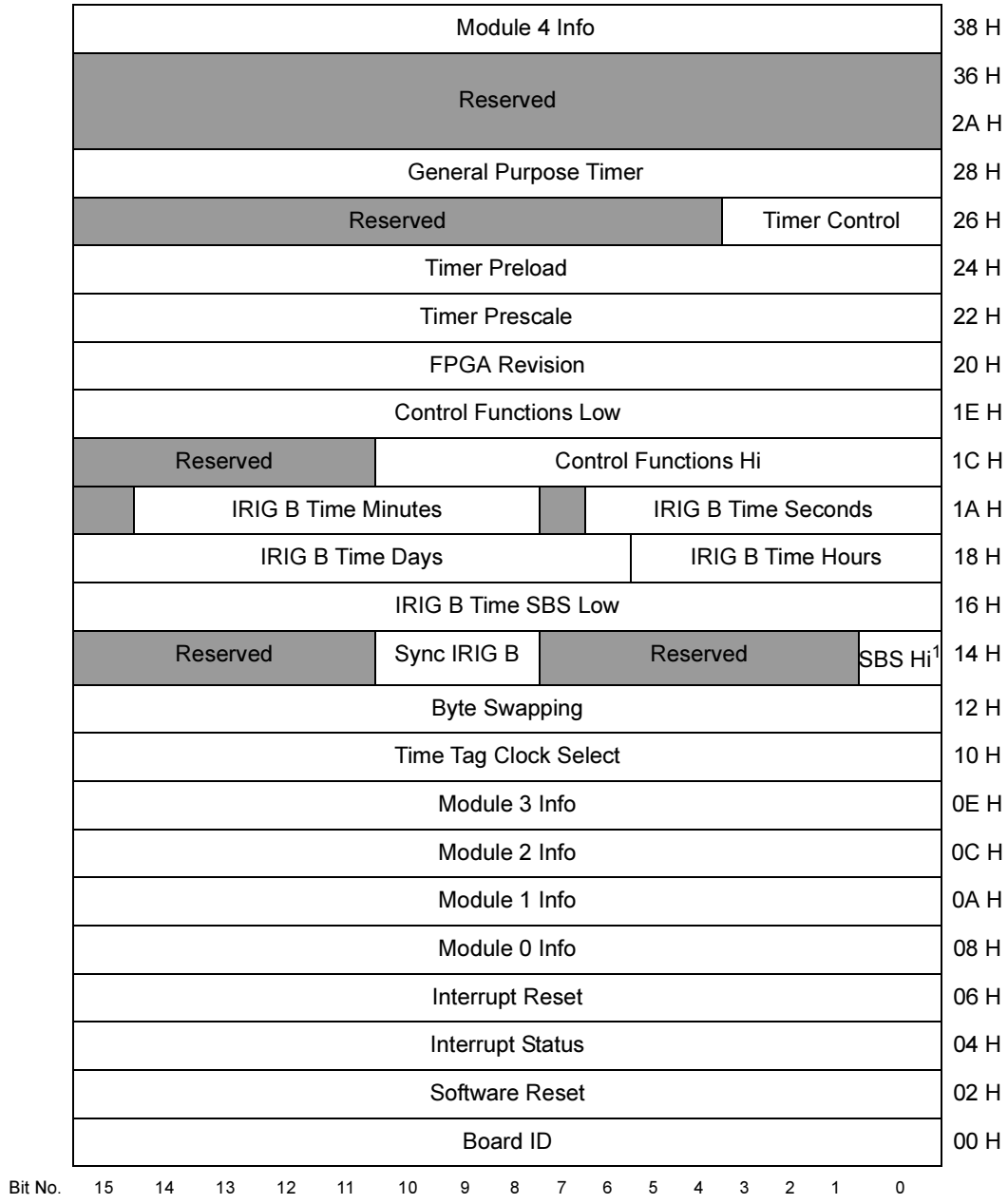

Figure 2-3 *EXC-4000P104plus* Global and IRIG B Registers Map

1. IRIG B Time SBS Hi Register

2.5.1 Board Identification Register

Address: 00 (H)
Length 16 bits

Read only

The Board Identification register is comprised of two identification items.

Bit	Description
04-15	Hard coded to the value 400 H
02-03	Hard coded to 00 H
00-01	Selected ID See section **3.3.1 Selected ID/ PC/104-Plus Slot ID Jumpers [JP1, JP2],** on page 3-3.

Board Identification Register

2.5.2 Software Reset Register

Address: 02 (H)
Length 16 bits

Write only

The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the modules Time Tag counters.

Bit	Description	
06-15	Reserved – set to 0	
05	Module 4 reset	1 = Reset module 0 = No effect
04	Global Time Tag reset	1 = Reset all Time Tag counters 0 = No effect
03	Module 3 reset	1 = Reset module 0 = No effect
02	Module 2 reset	1 = Reset module 0 = No effect
01	Module 1 reset	1 = Reset module 0 = No effect
00	Module 0 reset	1 = Reset module 0 = No effect

Software Reset Register

2.5.3 Interrupt Status Register

Address: 04 (H)
Length 16 bits

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
06-15	Reserved – set to 0
05	1 = Indicates that module 4 is interrupting
04	1 = Indicates that an interrupt was generated by the General Purpose Timer (See section **2.7 Global Timer Registers,** on page 2-16)
03	1 = Indicates that module 3 is interrupting
02	1 = Indicates that module 2 is interrupting
01	1 = Indicates that module 1 is interrupting
00	1 = Indicates that module 0 is interrupting

Interrupt Status Register

2.5.4 Interrupt Reset Register

Address: 06 (H)
Length 16 bits

Write only The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
06-15	Reserved – set to 0
05	1 = Resets module 4 interrupt 0 = No effect
04	1 = Resets General Purpose Timer interrupt 0 = No effect
03	1 = Resets module 3 interrupt 0 = No effect
02	1 = Resets module 2 interrupt 0 = No effect
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Interrupt Reset Register

2.5.5 Module Info [0-4] Registers

Address: 08, 0A, 0C, 0E, 38 (H)
Length 16 bits each

Read only The Module Info Registers provide identification information for each of the four modules, respectively.

Bit	Description	
12-15	Module ID	00 H = Module 0 Info register 01 H = Module 1 Info register 02 H = Module 2 Info register 03 H = Module 3 Info register 04 H = Module 4 Info register
05-11	Reserved – set to 0	
00-04	Module type	02 H = M4KSerial 03 H = M4K1553MCH module 04 H = M4K429RTx module 05 H = M4K1553Px module 06 H = M4KMMSI module 07 H = M4K708 module 08 H = M4K1553MA 0C H = M4KCAN module 0D H = M4KDiscrete module 1F H = no module installed

Module Info Registers

Note: 1. For Module 0, if installed, the Module type is fixed to a value of 04 H.
2. For Module 3 and Module 4, if installed, the Module type is fixed at 05 H.

2.5.6 Time Tag Clock Select Register

Address: 10 (H)
Length 16 bits

Read/Write The Time Tag Clock Select Register is used to set either an internal (1 MHz) or external source for the board's Global Time Tag Clock. See section **3.4.6 External Signals Connector J7,** on page 3-21, for details of the External Time Tag Clock.

Bit	Description	
01-15	Reserved – set to 0	
00	Time Tag Clock Select	1 = External Source 0 = Internal Source (**Default**)

Time Tag Clock Select Register

2.5.7 Byte Swapping

Address: 12 (H)
Length 16 bits

Read/Write The Byte Swapping Register may be used to swap the high byte with the low byte of the module memory space and the global registers on the *EXC-4000P104plus*. This may be useful on some host computers that byte-swap their memory.

Bit	Description	
00-15	A1A1	Enable byte swapping
	Any other value	Disable byte swapping **(Default)**

Byte Swapping Register

2.6 IRIG B Global Registers

The *EXC-4000P104plus* is able to receive and decode standard serial IRIG B time code format signals (1 KHz carrier wave, sine wave - amplitude modulated, 100 peaks per second) via its External Signal Connector J2. See section **3.4.6 External Signals Connector J7,** on page 3-21.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the modules on the *EXC-4000PCI*.

1st Word	Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.
2nd Word	Set of bits reserved for decoding various control, identification and other special purpose functions.
3rd Word	Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 14 - 1E (H).

See **Figure 2-3 EXC-4000P104plus Global and IRIG B Registers Map,** on page 2-9 for the location of the registers on the memory map.

Note:

- The IRIG B design is based on the Global Time Tag Clock. This clock has a default value of 1MHz. If the **Time Tag Clock Select Register** is set to 1 (external source), the user *must* ensure that the external source be set to 1MHz, otherwise the IRIG B register will not record the correct value of the IRIG message received.
- The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.
- See **Time Tag Clock Select Register,** on page 2-12 and **3.4.6.1 External Signals Descriptions [Connector J7],** on page 3-21.

2.6.1 Sync IRIG B Register

Address: 14 (H)
Bits 08 – 10

Read/Write The 3-bit Sync IRIG B register controls the synchronization of a module's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B time registers.

Bit		Description
10	1	Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers
	0	No IRIG B time has been stored in the IRIG B registers. This bit must be reset by the user after the board has written a "1".
09	1	Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (14-1E (H)) corresponding to the next valid IRIG B message (the time to which the Time Tags of all the modules are synchronized.)
	0	The next valid IRIG B message should not be stored in the IRIG B registers. This bit will be automatically reset by the board after the storage of the IRIG B time.
08	1	Resets and synchronizes Time Tags of all the modules to the next rising edge of the on-time Reference Point **Pr** of the IRIG B signal. Also sets Bit 09 to a value of "1" in order to store and display the IRIG B time and control functions into the 6 IRIG B registers. The value stored represents the time to which the Time Tags are synchronized to, delayed by one second.
	0	No reset/synchronization of Time Tags relative to the **Pr** of the IRIG B signal. This bit will be automatically reset by board after reset of Time Tags

Sync IRIGB Register

Note: All bits are read and write.

2.6.2 IRIG B Time SBS High Register

Address: 14 (H)
Bit 0

Read only The IRIG B Time SBS High register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.3 IRIG B Time SBS Low Register

Address: 16 (H)
Bits 15 – 0

Read only The IRIG B Time SBS Low register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.4 IRIG B Time Days Register

Address: 18 (H)
Bits 15 – 6

Read only The IRIG B Time Days register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

2.6.5 IRIG B Time Hours Register

Address: 18 (H)
Bits 5 – 0

Read only The IRIG B Time Hours register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.

2.6.6 IRIG B Time Minutes Register

Address: 1A (H)
Bits 14 – 8

Read only The IRIG B Time Minutes register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.

2.6.7 IRIG B Time Seconds Register

Address: 1A (H)
Bits 6 – 0

Read only The IRIG B Time Seconds register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.

2.6.8 Control Functions Registers

Hi Register Address: 1C (H) / Bits 10 – 0
Low Register Address: 1E (H) / Bits 15 – 0

Read only The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.

2.6.9 FPGA Revision Register

Address: 20 (H)
Bits 15 – 0

Read only The FPGA Revision register contains the FPGA revision of the board.

2.7 Global Timer Registers

See **Figure 2-3 EXC-4000P104plus Global and IRIG B Registers Map,** on page 2-9 for location of the registers on the memory map.

2.7.1 Timer Prescale Register

Address: 22 (H)
Bits 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.7.2 Timer Preload Register

Address: 24 (H)
Bits 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.7.3 Timer Control Register

Address: 26 (H)
Bits 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1	Causes global reset of all installed modules
		0	No effect
02	Interrupt on count completed	1	Output an interrupt (see **2.5.3 Interrupt Status Register,** on page 2-11)
		0	No effect
01	Reload mode	1	Reload mode
		0	Non-reload/One-shot mode
00	Start/Stop	1	Start
		0	Sop

Timer Control Register

2.7.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value

will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-4000P104plus* carrier board.

3.1 *EXC-4000P104plus* Board Layout

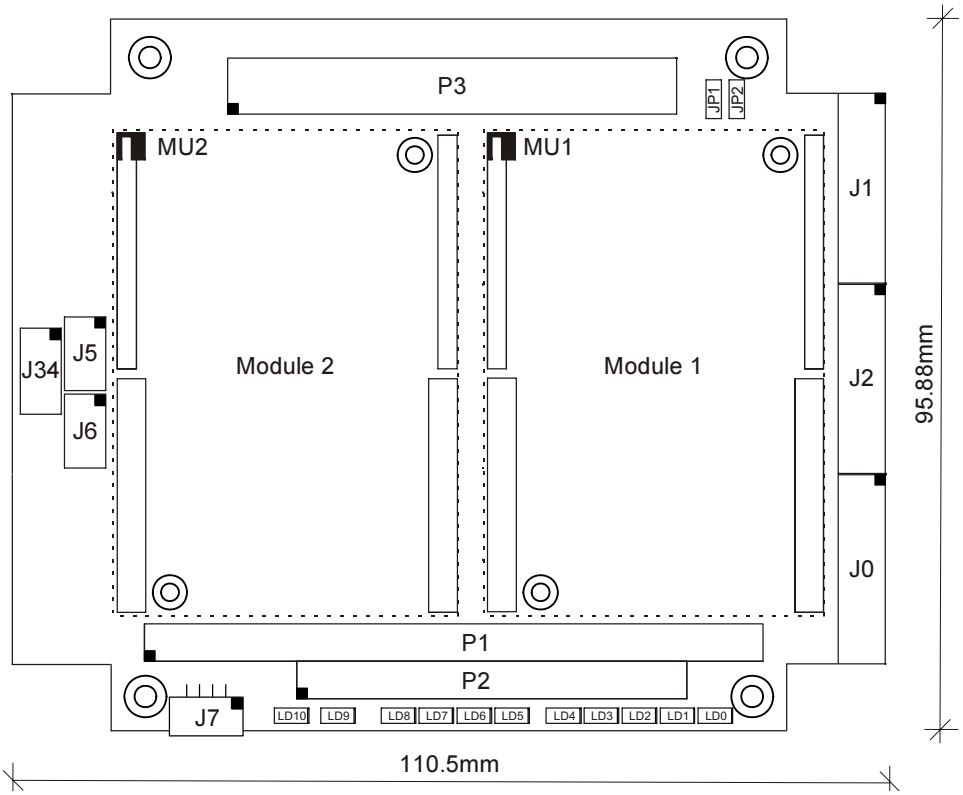

Figure 3-1 *EXC-4000P104plus* Board Layout – Top View

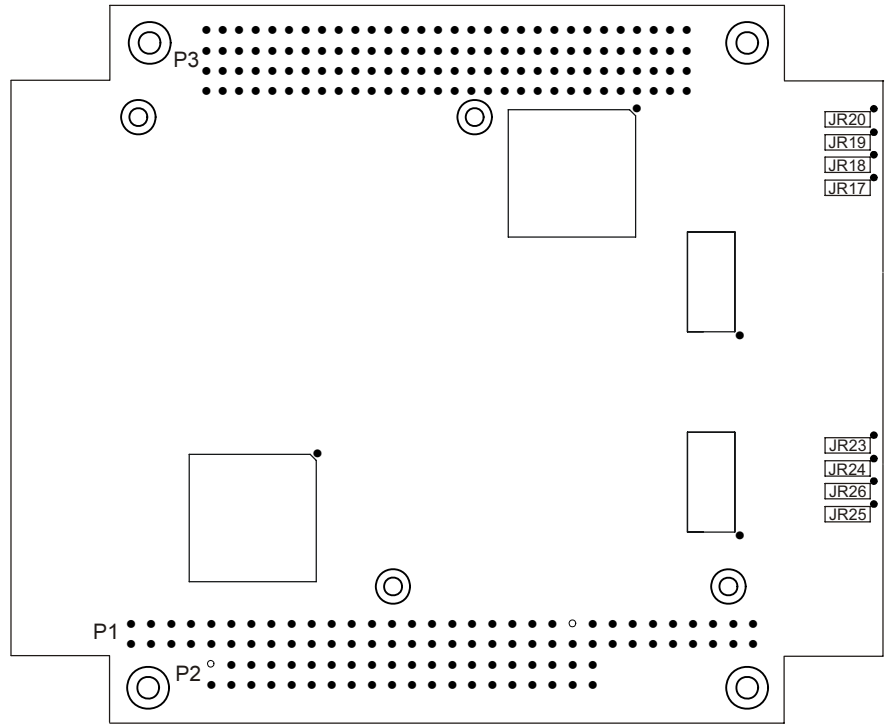

Figure 3-2 *EXC-4000P104plus* Board Layout – Bottom View

Note: Modules 0 (ARINC 429) is integrated directly on the PCB on the top side of the board under Module 1.
Module 3 and Module 4 (MIL-STD-1553) are integrated directly on the PCB on the reverse side of the board.

3.2 Led Indicators

The *EXC-4000P104plus* contains ten LEDs.

LED	Indication
LD0	Module 0 ready
LD1	Module 1 ready
LD2	Module 2 ready
LD3	Module 3 ready
LD4	Module 4 ready
LD5	Module 0 receive activity on channels 0 – 4
LD6	Module 0 transmit activity on channels 0 – 4
LD7	Module 0 receive activity on channels 5 – 9
LD8	Module 0 transmit activity on channels 5 – 9
LD9	Module 3 bus activity
LD10	Module 4 bus activity

Led Indicators

3.3 Jumpers

The *EXC-4000P104plus* contains the following sets of jumpers:

- Selected ID/ PC/104-*Plus* slot ID jumpers
- Module 3 (1553 Px) Coupling Mode select jumpers
- Module 4 (1553 Px) Coupling Mode select jumpers

3.3.1 Selected ID/ PC/104-*Plus* Slot ID Jumpers [JP1, JP2]

The Selected ID/PC-104-*Plus* slot ID Jumpers serve two purposes:

- To define the "Select ID' of the board within the Global Registers – see section **2.5.1 Board Identification Register** on page 2-10;
- To define the PC/104-*Plus* slot ID number. This number defines a unique identification for the *EXC-4000P104plus* relative to the other boards in the PC/104-*Plus* computer. The *EXC-4000P104plus* Slot ID number *must* be different from any other boards in the PC/104-*Plus* computer.

The two through hole jumpers represent a two bit digit of which JP2 is the most significant bit. When a jumper is

- **Not Installed** a value of "1" will be set for that bit
- **Installed** a value of "0" will be set for that bit

Multiple Board Applications

To provide a unique 'Selected ID', to identify a board by the application software in a multiple board application, the jumpers should be set differently for each board. For example:

Board	ID#1	ID#3
Bit 0 [JP1]	Not Installed	Not Installed
Bit 1 [JP2]	Installed	Not Installed

JP1 & JP2 settings for unique 'Selected ID'

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the 'unique ID' to match the value represented by the "Selected ID" Jumpers.

Selected ID	Bit 1	Bit 0
0	Installed	Installed
1	Installed	Not Installed
2	Not Installed	Installed
3	Not Installed	Not Installed

Jumper Settings for Unique "Selected ID"

3.3.1.1 Factory Default Jumper Settings

The factory default jumper settings are:

Jumper	Status
JP1	Not Installed
JP2	Not Installed

Factory Default Jumper Settings

3.3.2 Module 3 and 4 (1553 Px) Coupling Mode Select Jumpers [JR17 – JR20, JR23 – JR26]

The Module 3 and Module 4 (1553 Px) Coupling Mode select jumpers control the onboard 1553 interfaces (Direct/ Transformer coupled). These jumpers are surface mounted 0 Ohm resistors that are soldered on to the board, according to the default board setup. (See section **3.3.2.1 Factory Default Jumper Settings**). If different Jumper settings are required, the 0 Ohm register will have to be removed and either a 0 Ohm resistor or a wire will have to be soldered in the desired position.

The Module 3 and Module 4 (1553 Px) can be either direct-coupled or transformer-coupled to the 1553 bus. (See **1553 Bus Connections** in the *M4K1553Px User's Manual*).

Table **3-1** defines the Jumper settings for all eight Jumpers.

Coupling Mode	Setting
Transformer-Coupled	Short pins 1 and 2
Direct-Coupled	Short pins 2 and 3

Table 3-1 Jumper Settings Required to Select Coupling Mode

Table **3-2** defines the Jumper for each bus.

Module	Bus	Jumper Group
3	A	JR17, JR 18
	B	JR19, JR 20
4	A	JR23, JR 24
	B	JR25, JR26

Table 3-2 Jumper Groups

3.3.2.1 Factory Default Jumper Settings

The factory default settings are:

Jumper Type	Jumpers	Pin #	Description
3-pin	JR17 – JR 20 JR23 – JR 26	Pins 1 and 2 (0 Ohm resistor installed)	Transformer coupled mode

Table 3-3 Factory Default Jumper Settings

3.4 Connectors

The *EXC-4000P104plus* board contains the following connectors:

1. A **24-pin, 2mm double-row socket header connector** [J0] passes all of Module 0 (ARINC 429) I/O signals:
   P/N **HRS ® DF11-24DP-2DSA**

   A mating connector is provided:
   P/N **HRS ® DF11-24DS-2C** – Housing
   P/N **HRS ® DF11-2428SCA** – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.1.1 J0 Connector Pinouts (ARINC 429)**, on page 3-7. Note that the J0 pinouts differ from J1/J2 when an ARINC 429 module is installed in module locations 1 or 2.

2. Two **2mm double-row socket header connectors** [J1] and [J2] pass all of modules 1 and 2 (multiprotocol) I/O signals:
   P/N **HRS ® DF11-24DP-2DSA**

   Mating connectors are provided:
   P/N **HRS ® DF11-24DS-2C** – Housing
   P/N **HRS ® DF11-2428SCA** – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.2.1 J1 and J2 Connector Pinouts (Multiprotocol)**, on page 3-9.

3. A **10-pin, 2mm double-row socket header connector** [J34] passes all of Module 3 (1553 Px) and Module 4 (1553 Px) I/O signals:
   P/N **HRS ® DF11-10DP-2DSA**

   A Mating connector is provided:
   P/N **HRS ® DF11-10DS-2C** – Housing
   P/N **HRS ® DF11-2428SCA** – Crimp terminal pins

For a description of the connector pinouts and signals, see section **3.4.3.1 J34 Connector Pinouts (MIL-STD-1553)**, on page 3-18.

4. Two **8-pin, 2mm double-row socket header connectors** [J5] and [J6] pass the 1553 RT address signals for modules 3 and 4:
P/N **HRS ® DF11-8DP-2DSA**

   Mating connectors are provided when ordering a board with an onboard single function (*PxS*) module in module locations 3 or 4:
P/N **HRS ® DF11-8DS-2C** – Housing
P/N **HRS ® DF11-2428SCA** – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.4.1 J5 and J6 Connector Pinouts (1553 RT Address Signals)**, on page 3-19.

5. A **120-pin, elevated socket strip PC/104-*Plus* connector**, centerline 2mm [P3] passes all of the PCI I/O signals:
P/N **Samtec ® ESQT-130-02-G-Q-368**

   A 120-pin plastic shroud is provided as an optional cover to protect the pins of the PC/104-*Plus* connector [P3]:
P/N **Samtec ® ATS-30-Q**

   For a description of the connector pinouts and signals, see section **3.4.5 PCI Bus I/O Connector [P3]**, on page 3-20.

6. An **8-pin, male connector** [J7] provides all the external signals:
P/N **Molex ® 87333-0831**

   A mating crimp housing and crimp terminals are provided:
P/N **Molex ® 51110–0860** – Housing
P/N **Molex ® 50394–8100** – Crimp terminal pins

   For a description of the connector pinouts and signals, see section **3.4.6.1 External Signals Descriptions [Connector J7]**, on page 3-21.

7. An **64-pin, PC/104 (ISA) connector** [P1].
8. An **48-pin, PC/104 (ISA) connector** [P2].

   The **64-pin** and **48-pin PC/104** connectors are used for stack-through purposes and have no signals connected to them.

3.4.1 Module 0 (ARINC 429) Communications I/O Connector [J0]

The **24-pin, 2mm double-row socket header** passes all the relevant signals associated with Module 0 (ARINC 429) to the connected ARINC 429 bus.

Note: J0 pinouts differ from J1/J2 when an ARINC 429 module is installed in module locations 1 or 2.

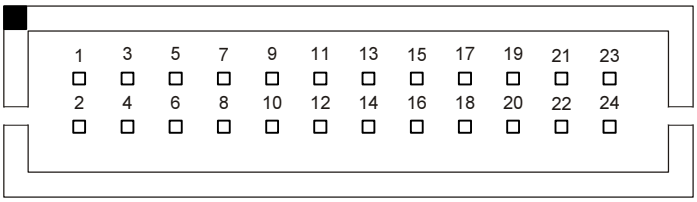

Figure 3-3 J0 Connector Layout – Top View

3.4.1.1 J0 Connector Pinouts (ARINC 429)

J0 Pin #	Signal Name	Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the mechanical holes.
2	GND	Provides ground reference for the OUTRIGn output.
3	M0CH0L	Channel 0 ARINC low line connection
4	M0CH0H	Channel 0 ARINC high line connection
5	M0CH1L	Channel 1 ARINC low line connection
6	M0CH1H	Channel 1 ARINC high line connection
7	M0CH2L	Channel 2 ARINC low line connection
8	M0CH2H	Channel 2 ARINC high line connection
9	M0CH3L	Channel 3 ARINC low line connection
10	M0CH3H	Channel 3 ARINC high line connection
11	M0CH4L	Channel 4 ARINC low line connection
12	M0CH4H	Channel 4 ARINC high line connection
13	M0CH5L	Channel 5 ARINC low line connection
14	M0CH5H	Channel 5 ARINC high line connection
15	M0CH6L	Channel 6 ARINC low line connection
16	M0CH6H	Channel 6 ARINC high line connection
17	M0CH7L	Channel 7 ARINC low line connection
18	M0CH7H	Channel 7 ARINC high line connection
19	M0CH8L	Channel 8 ARINC low line connection
20	M0CH8H	Channel 8 ARINC high line connection
21	M0CH9L	Channel 9 ARINC low line connection
22	M0CH9H	Channel 9 ARINC high line connection
23	M0OUTRIGn	This low active output provides trigger pulses of approximately 400 nsec. width and is activated under software control upon the same conditions as interrupts. See Interrupt/ Trigger Conditions Registers in the *M4K429RTx User's Manual.* This output is an open-collector with 330-ohm pull-up resistor to +3.3V
24	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the mechanical holes.

Table 3-4 J0 Connector Pinouts (ARINC 429)

3.4.2 Modules 1 and 2 (Multiprotocol) Communications Connector [J1, J2]

The two **24-pin, 2mm double-row socket headers** pass all the relevant signals associated with Module 1 [J1] (multiprotocol) and Module 2 [J2] (multiprotocol) to the connected buses.

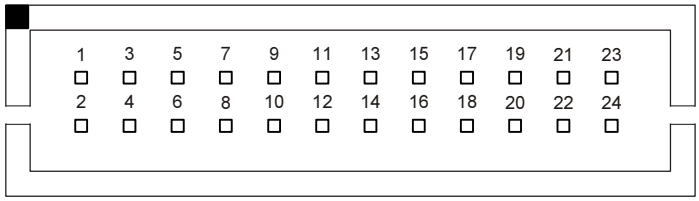

Figure 3-4 J1 and J2 Connector Layout – Top View

3.4.2.1 J1 and J2 Connector Pinouts (Multiprotocol)

The pinouts of J1 and J2 vary depending on the modules installed in module locations 1 and 2. The following tables list the pinouts for each module type.

J1/J2 Connector Pinouts for *M4K1553Px* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer.
2	BUSALO	1553 Bus A low connection.
3	BUSAHI	1553 Bus A high connection.
4 – 9	Reserved	Do not use this pin.
10	BUSBLO	1553 Bus B low connection.
11	BUSBHI	1553 Bus B high connection.
12	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer.
013	RTA0	Single function module (*PxS*) RT address bit position 0 input[1].
14	RTA1	Single function module (*PxS*) RT address bit position 1 input[1].
15	RTA2	Single function module (*PxS*) RT address bit position 2 input[1].
16	RTA3	Single function module (*PxS*) RT address bit position 3 input[1].
17	RTA4	Single function module (*PxS*) RT address bit position 4 input[1].
18	RTPTY	Single function module (*PxS*) RT address parity bit input[1].
19	RTLOCKn	Single function module (*PxS*) RT address lock input[1]. 0 = RT number locked (RT address is set to the value represented by pins 13 – 18) 1 = RT number unlocked (RT address can be changed by writing to the RT Number Register)
20	GND	Provided for single function module (*PxS*) RT address pins that need to be set to '0.'
21 – 22	Reserved	Do not use this pin.
23	EXSTARTn	External Start LVTTL input. Provides an option to start the module externally by applying a negative pulse with respect to the GND pin, with a minimum width of 100 nsec. Before applying the pulse, the module should be fully set up in the required mode, except the Start register bit 00, which should be left at 0. To stop the selected operation, follow the normal procedure described under the Start register.
24	GND	Provides ground reference for the digital signal connections.

Table 3-5 J1/J2 Connector Pinouts for *M4K1553Px* Modules

1. Single function module (*PxS*) only;
   Pin shorted to ground = logic 0
   Pin open = logic 1
   See the RT Number Register in the *M4K1553Px Module User's Manual*.

J1/J2 Connector Pinouts for *M4KMCH* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
2	BUSALO	1553 Bus A low connection
3	BUSAHI	1553 Bus A high connection
4 – 9	N/C	Not connected
10	BUSBLO	1553 Bus B low connection
11	BUSBHI	1553 Bus B high connection
12	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
13 – 23	N/C	Not connected
24	GND	Provides ground reference for the digital signal connections

Table 3-6 J1/J2 Connector Pinouts for *M4K1553MCH* Modules

J1/J2 Connector Pinouts for *M4K429RTx* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0L	ARINC 429 Channel 0 low connection
3	CH0H	ARINC 429 Channel 0 high connection
4	CH1L	ARINC 429 Channel 1 low connection
5	CH1H	ARINC 429 Channel 1 high connection
6	CH2L	ARINC 429 Channel 2 low connection
7	CH2H	ARINC 429 Channel 2 high connection
8	CH3L	ARINC 429 Channel 3 low connection
9	CH3H	ARINC 429 Channel 3 high connection
10	CH4L	ARINC 429 Channel 4 low connection
11	CH4H	ARINC 429 Channel 4 high connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH5L	ARINC 429 Channel 5 low connection
14	CH5H	ARINC 429 Channel 5 high connection
15	CH6L	ARINC 429 Channel 6 low connection
16	CH6H	ARINC 429 Channel 6 high connection
17	CH7L	ARINC 429 Channel 7 low connection
18	CH7H	ARINC 429 Channel 7 high connection
19	CH8L	ARINC 429 Channel 8 low connection
20	CH8H	ARINC 429 Channel 8 high connection
21	CH9L	ARINC 429 Channel 9 low connection
22	CH9H	ARINC 429 Channel 9 high connection
23	OUTRIGn	This low active output provides trigger pulses of approximately 400 nsec. width and is activated under software control upon the same conditions as interrupts. See Interrupt/ Trigger Mask Registers. This output is an open-collector with 330-ohm pull-up resistor.
24	GND	Provides ground reference for the OUTRIGn output.
	N/C	Not connected

Table 3-7 J1/J2 Connector Pinouts for *M4K429RTx* Modules

J1/J2 Connector Pinouts for *M4KDiscrete* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	IO0	Discrete 0
2	IO1	Discrete 1
3	IO2	Discrete 2
4	IO3	Discrete 3
5	IO4	Discrete 4
6	IO5	Discrete 5
7	IO6	Discrete 6
8	GND	Provides ground reference for input and output channels
9	IO7	Discrete 7
10	IO8	Discrete 8
11	EXT_TRIG	TTL Active low External trigger (pulse width approx. 150 nS)
12	SHIELD	Provides the input and output channels with shield connections. This signal is connected to the case of the computer.
13	IO9	Discrete 9
14	IO10	Discrete 10
15	IO11	Discrete 11
16	IO12	Discrete 12
17	IO13	Discrete 13
18	IO14	Discrete 14
19	IO15	Discrete 15
20	IO16	Discrete 16
21	GND	Provides ground reference for input and output channels
22	IO17	Discrete 17
23	IO18	Discrete 18
24	IO19	Discrete 19
	N/C	Not connected

Table 3-8 J1/J2 Connector Pinouts for *M4KDiscrete* Modules

J1/J2 Connector Pinouts for *M4KSerial* Modules

J1/J2 Pin #	Signal Name	Signal Description		
		RS-232	RS-485	RS-422
1	Reserved	Do not use this pin.		
2	485/422T_0	N/C	Channel 0 high connection	Channel 0 Transmit high connection
3	232T/485n/422Tn_0	Channel 0 Transmit connection	Channel 0 low connection	Channel 0 Transmit low connection
4	232R/422R_0	Channel 0 Receive connection	N/C	Channel 0 Receive high connection
5	422Rn_0	N/C	N/C	Channel 0 Receive low connection
6	GND	Provides ground reference	N/C	N/C
7	Reserved	Do not use this pin.		
8	485/422T_1	N/C	Channel 1 high connection	Channel 1 Transmit high connection
9	232T/485n/422Tn_1	Channel 1 Transmit connection	Channel 1 low connection	Channel 1 Transmit low connection
10	232R/422R_1	Channel 1 Receive connection	N/C	Channel 1 Receive high connection
11	422Rn_1	N/C	N/C	Channel 1 Receive low connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.		
13	485/422T_2	N/C	Channel 2 high connection	Channel 2 Transmit high connection
14	232T/485n/422Tn_2	Channel 2 Transmit connection	Channel 2 low connection	Channel 2 Transmit low connection
15	232R/422R_2	Channel 2 Receive connection	N/C	Channel 2 Receive high connection
16	422Rn_2	N/C	N/C	Channel 2 Receive low connection
17	GND	Provides ground reference	N/C	N/C
18	Reserved	Do not use this pin.		
19	485/422T_3	N/C	Channel 3 high connection	Channel 3 Transmit high connection
20	232T/485n/422Tn_3	Channel 3 Transmit connection	Channel 3 low connection	Channel 3 Transmit low connection
21	232R/422R_3	Channel 3 Receive connection	N/C	Channel 3 Receive high connection
22	422Rn_3	N/C	N/C	Channel 3 Receive low connection
23	Reserved	Do not use this pin.		
24	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.		
	N/C	Not connected	Not connected	Not connected

Table 3-9 J1/J2 Connector Pinouts for *M4KSerial* Modules

J1/J2 Connector Pinouts for *M4KCAN* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
2	CAN0H	Channel 0 high connection
3	CAN0L	Channel 0 low connection
4	CAN1H	Channel 1 high connection
5	CAN1L	Channel 1 low connection
6	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
7	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
8	CAN2H	Channel 2 high connection
9	CAN2L	Channel 2 low connection
10	CAN3H	Channel 3 high connection
11	CAN3L	Channel 3 low connection
12	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
13	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
	N/C	Not connected
14	CAN4H	Channel 4 high connection
15	CAN4L	Channel 4 low connection
16	CAN5H	Channel 5 high connection
17	CAN5L	Channel 5 low connection
18	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
19	Reserved	Do not use this pin.
20	Reserved	Do not use this pin.
21	GND	Provides ground reference
22	N/C	Not connected
23	N/C	Not connected
24	N/C	Not connected

Table 3-10 J1/J2 Connector Pinouts for *M4KCAN* Modules

J1/J2 Connector Pinouts for *M4K708* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	BUS0L	Channel 0 low connection
3	BUS0H	Channel 0 high connection
4 – 9	N/C	Not connected
10	BUS1L	Channel 1 low connection
11	BUS1H	Channel 1 high connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13 – 18	N/C	Not connected
19 – 22	Reserved	Do not use this pin.
23	OUTRIGn	Output trigger low active output. Provides trigger pulses of approximately 500 nsec. width and is activated upon the same conditions as interrupts. See Channel Output Trigger Mask Register in the *M4K708 Module User's Manual*. This output is an open-collector type pulled up with a 330-Ohm resistor to 5V.
24	GND	Provides ground reference for the OUTRIGn output.

Table 3-11 J1/J2 Connector Pinouts for *M4K708* Modules

J1/J2 Connector Pinouts for *M4KMMSI* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0L	Port 0 low connection
3	CH0H	Port 0 high connection
4	CH1L	Port 1 low connection
5	CH1H	Port 1 high connection
6	CH2L	Port 2 low connection
7	CH2H	Port 2 high connection
8	CH3L	Port 3 low connection
9	CH3H	Port 3 high connection
10	CH4L	Port 4 low connection
11	CH4H	Port 4 high connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH5L	Port 5 low connection
14	CH5H	Port 5 high connection
15	CH6L	Port 6 low connection
16	CH6H	Port 6 high connection
17	CH7L	Port 7 low connection
18	CH7H	Port 7 high connection
19	CH8L	Composite BM Output low connection
20	CH8H	Composite BM Output high connection
21	N/C	Not connected
22	N/C	Not connected
	N/C	Not connected
23	EXSTRTn	External Start TTL input. Provides an option to start the module externally by applying a negative pulse of 100 nsec/min. with respect to the GND pin. Before applying the pulse, the module should be fully set up in the required mode, except the Start register bit 00, which should be left at 0. To stop the selected operation, follow the normal procedure described under the Start register.
24	GND	Provides ground reference for the EXSTRTn signal

Table 3-12 J1/J2 Connector Pinouts for *M4KMMSI* Modules

J1/J2 Connector Pinouts for *M4KH009* Modules

J1/J2 Pin #	Adapter Cable Connector (Twinax)	Signal Name	Signal Description
1	BODY ASSEMBLY	SHIELD	Provided for H009 cables shield connection. This signal is connected to the case of the computer
2	INNER SHEATH	DBUSAL	Bus A Data low connection
3	CENTER PIN	DBUSAHI	Bus A Data high connection
4	INNER SHEATH	DBUSBL	Bus B Data low connectionv
5	CENTER PIN	DBUSBHI	Bus B Data high connection
6	INNER SHEATH	CBUSAL	Bus A Clock low connection
7	CENTER PIN	CBUSAHI	Bus A Clock high connection
8	INNER SHEATH	CBUSBL	Bus B Clock low connection
9	CENTER PIN	CBUSBHI	Bus B Clock high connection
10 – 11		GND	Provides ground reference for digital signal connections
12	BODY ASSEMBLY	SHIELD	Provided for H009 cables shield connection. This signal is connected to the case of the computer
13 – 21		N/C	Not connected
22		Reserved	Do not use this pin.
23 – 24		GND	Provides ground reference for digital signal connections

Table 3-13 J1/J2 Connector Pinouts for *M4KH009* Modules

3.4.3 Modules 3 and 4 (MIL-STD-1553) Communications I/O Connector [J34]

The **10-pin, 2mm double-row socket header** connector passes all the relevant signals associated with Module 3 (1553 Px) and Module 4 (1553 Px) to the connected MIL-STD-1553 bus.

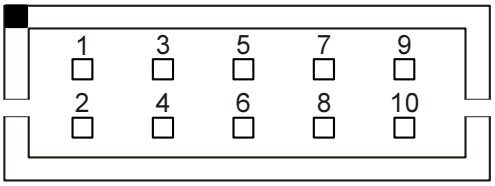

Figure 3-5 J34 Connector Layout – Top View

3.4.3.1 J34 Connector Pinouts (MIL-STD-1553)

J34 Pin #	Signal Name	Description
1	M3BUSAH	Module 3 Bus A connection Hi
2	M3BUSAL	Module 3 Bus A connection Lo
3	M3BUSBH	Module 3 Bus B connection Hi
4	M3BUSBL	Module 3 Bus B connection Lo
5	SHIELD	Provided for MIL-STD-1553 cables shield connection. This signal is connected to the case of the computer.
6	SHIELD	Provided for MIL-STD-1553 cables shield connection. This signal is connected to the case of the computer.
7	M4BUSAH	Module 4 Bus A connection Hi
8	M4BUSAL	Module 4 Bus A connection Lo
9	M4BUSBH	Module 4 Bus B connection Hi
10	M4BUSBL	Module 4 Bus B connection Lo

Table 3-14 J34 Connector Pinouts (MIL-STD-1553)

3.4.4 Modules 3 and 4 1553 RT Address Signals Connectors [J5, J6]

Two **8-pin, 2mm double-row socket header** connectors pass the 1553 RT address signals for Module 3 [J5] and Module 4 [J6].

Note: J5/J6 are only used when Module 3 and/or Module 4 are single function *M4K1553PxS* modules.

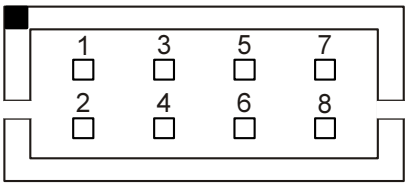

Figure 3-6 J5 and J6 Connector Layout – Top View

3.4.4.1 J5 and J6 Connector Pinouts (1553 RT Address Signals)

J5/J6 Pin #	Signal Name	Description
1	RTA0	Single function module (*PxS*) RT address bit position 0 input[1]
2	RTA1	Single function module (*PxS*) RT address bit position 1 input[1]
3	RTA2	Single function module (*PxS*) RT address bit position 2 input[1]
4	RTA3	Single function module (*PxS*) RT address bit position 3 input[1]
5	RTA4	Single function module (*PxS*) RT address bit position 4 input[1]
6	RTPTY	Single function module (*PxS*) RT address parity bit input[1]
7	RTLOCKn	Single function module (*PxS*) RT address lock 0 = RT number locked (RT address is set to the value represented by pins 13 – 18) 1 = RT number unlocked (RT address can be changed by writing to the RT Number Register)
8	GND	Provided for single function module (*PxS*) RT address pins that need to be set to '0'

Table 3-15 J5 and J6 Connector Pinouts (1553 RT Address Signals)

1. Pin shorted to ground = logic 0
   Open = logic 1
   See **RT Number Register** in the *M4K1553Px Module User's Manual.*

3.4.5 PCI Bus I/O Connector [P3]

The standard PC/104-*Plus* connector passes all the relevant PCI signals to the *EXC-4000P104plus*.

Pin#	P3			
	A	B	C	D
1	N/C	N/C	+5V	AD00
2	N/C	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	N/C	AD10	N/C
7	AD14	AD13	GND	AD12
8	N/C	C/BE1#	AD15	N/C
9	SERR#	GND	N/C	PAR
10	GND	PERR#	N/C	N/C
11	STOP#	N/C	LOCK#	GND
12	N/C	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	N/C
14	GND	AD16	N/C	C/BE2#
15	AD18	N/C	AD17	GND
16	AD21	AD20	GND	AD19
17	N/C	AD23	AD22	N/C
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	N/C	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	N/C	GND	N/C	N/C
24	GND	N/C	+5V	N/C
25	N/C	N/C	N/C	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	N/C	+5V	RST#
29	+12V	INTA#	N/C	N/C
30	-12V	N/C	N/C	N/C

Table 3-16 PC/104-*Plus* Connector Pinouts [P3]

N/C = not connected

3.4.6 External Signals Connector J7

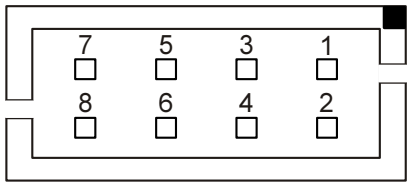

Figure 3-7 Connector J7 Pinouts – Front View

J7 Pin #	Signal Name	J7 Pin #	Signal Name
1	EXTTCLKI	**2**	EXTTRSTn
3	EXTTCLKO	**4**	GND
5	RESERVED	**6**	IRIG B
7	SHIELD	**8**	EXTTRSOn

Table 3-17 J7 Pinouts

3.4.6.1 External Signals Descriptions [Connector J7]

Signal	Description
EXTTCLKI	**External Time Tag Clock Input** (Nominal value: 1MHz). This signal supplies an external global clock for the Time Tags of all the modules. Use the signal to synchronize the Time Tags that are implemented on the modules[1] to other boards or systems.[2] See Time Tag Clock Select Register, page 2-12.
EXTTCLKO	**Global Time Tag Clock TTL Output** (1 MHz). This signal is the Global Clock that is supplied to all the modules for their Time Tags. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules.[1] The source of this clock is either the External Time Tag Clock **EXTTCLKI** [2] or the Internal Time Tag Clock. See Time Tag Clock Select Register, page 2-12
EXTTRSTn	**External Time Tag reset TTL Input** Use this low active pulsed signal (minimum 100 nsec.wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems.[2]
EXTTRSOn	**Global Time Tag Reset TTL Output** This low active signal is activated each time a Global Time Tag Reset is applied. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules.[1] This signal is activated by either the internal Global Time Tag signal See Software Reset Register, page 2-10 or from the External Time Tag signal (**EXTTRSOn**).[2]
IRIG B	**IRIG B Input** This should be a 1KHz sine wave, amplitude modulated, IRIG B signal with a 3:1 modulation ratio at 3V typical.
GND	Provides ground reference for the digital signal connections.
SHIELD	Provided for a cables shield connection. This signal is connected to the case of the computer through the mechanical holes.

Table 3-18 External Signals description [Connector J7]

1. See the manual for each module for a description of how the Time Tag clock is implemented, if used, for that module.

2. **To Synchronize with External Sources**

To synchronize a single *EXC-4000P104plus* board to an external system, the external clock source and the external reset must be connected to the **EXTTCLKI** and the **EXTTRSTn** signals respectively.

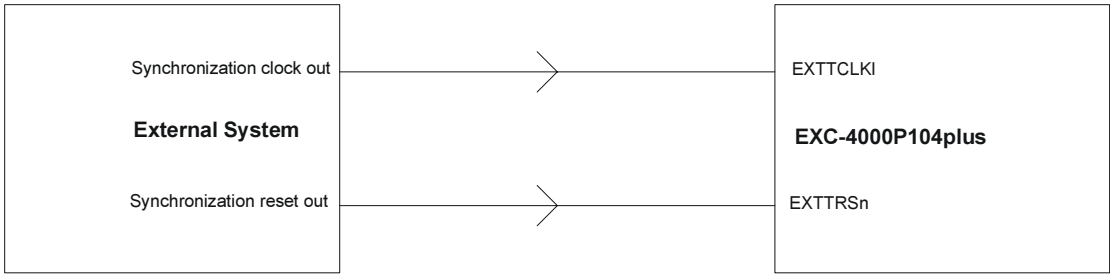

Figure 3-8 Synchronization of a Single *EXC-4000P104plus* Board to an External System

To synchronize an external system to a single *EXC-4000P104plus* board, the EXTTCLKO and the EXTTRSOn signals need to be connected to the external clock source and the external reset respectively.

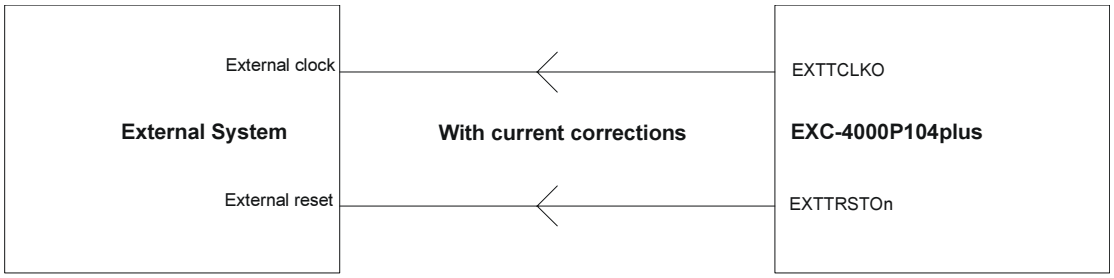

Figure 3-9 Synchronization of an External System to a Single *EXC-4000P104plus* Board

Warning: The synchronization clock and reset signals may be connected to multiple targets to achieve system wide synchronization.

To Synchronize Between *EXC-4000P104plus* Boards

To synchronize multiple *EXC-4000P104plus* boards the **EXTCLKO** and the **EXTTRSOn** signals of one board need to be connected to all the **ETTCLKI** and the **EXTTRSTn** signals respectively, of the remaining boards.

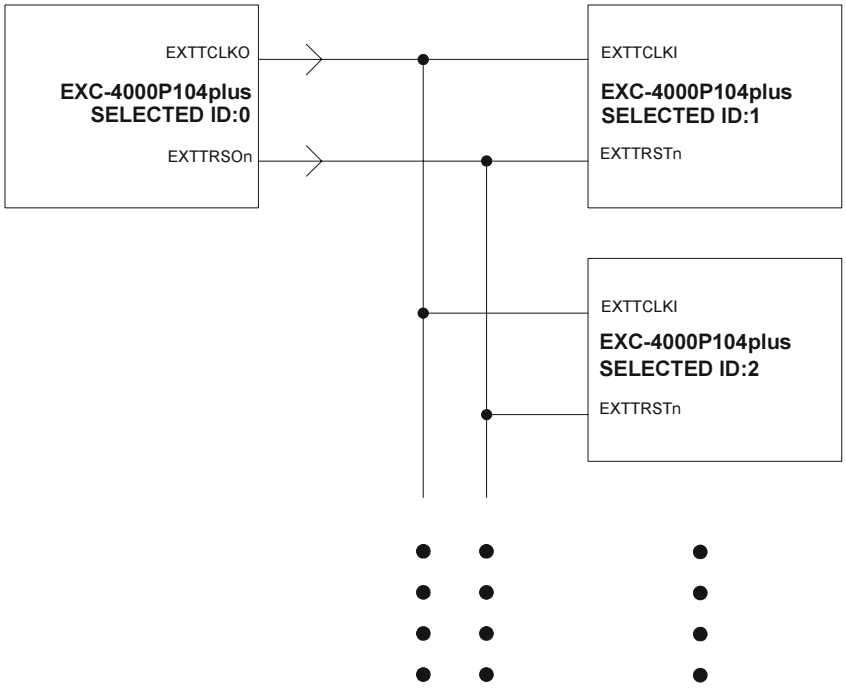

Figure 3-10 Synchronization Between *EXC-4000P104plus* Boards

3.5 Power Requirements

The recommended power requirements for the *EXC-4000P104plus* are:

- 170 mA @ +5 V for the base board only, not including any installed or onboard modules.
- For each onboard or installed module, add the power requirements listed in the *User's Manual* for that module.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering an *EXC-4000P104plus* carrier board.

Part Number	Option	Description
EXC-4000P104P/*$M_0M_1M_2M_3M_4$*		Multiprotocol interface board for PC/104-*Plus* compatible systems.
	-L	Add this suffix for the non-expandable version of the board. See the notes at the end of the ordering options for details.
	-001	Add this suffix for conformal coating.
	-E	Add this suffix for the extended temperature option (-40° to +85°C).

Table 4-1 Ordering Information

M_0, ***M_1***, ***M_2***, ***M_3*** and ***M_4*** represent the five module locations on the board. Module locations ***M_0***, ***M_3*** and ***M_4*** are spread modules soldered to the board. ***M_1*** and ***M_2*** are removable M4K modules.

- ***M_0*** can only be M4K429RT5 or M4K429RT10.
- ***M_1*** and ***M_2*** can be any of the M4K modules listed in the following table:
- ***M_3*** and ***M_4*** can only be M4K1553Px, M4K1553PxS, M4K1553PxM, M4K1553Px-1760 or M4K1553PxS-1760.

Module Code (for Ordering with Carrier Board)	Module Part # (for Ordering Separately)	Option	Description
A*x*	**M4K429RT5**		ARINC 429 interface module: supports up to five channels.
B*x*	**M4K429RT10**		ARINC 429 interface module: supports up to ten channels.
C*x*	**M4K708**		The module supports two ARINC 708/ 453 channels, each one selectable as either transmit or receive.
D*x*	**M4KH009**		Double-sized H009 interface module (occupies two module locations): supports CCC, multi-PU, CCC/ Concurrent PU and Bus monitor modes. Includes Concurrent Bus monitor mode.
E*x*	**M4K1553MCH**		MIL-STD-1553 interface single function module: supports BC, single RT, RT/ Concurrent-BM and BM modes. (Legacy product. For new systems, use the M4K1553PxS instead. The M4K1553MCH module is not available for PCI Express-based carrier boards.)
F*x* (or G*x*)	**M4K1553Px**		MIL-STD-1553 interface module: supports BC, multiple RTs, BC/ Concurrent-RT and Bus Monitor modes. Supports an Internal Concurrent Monitor in RT and BC/RT modes.

Table 4-2 M4K Module Codes and Part Numbers

Module Code (for Ordering with Carrier Board)	Module Part # (for Ordering Separately)	Option	Description
H*x*	**M4K1553PxS-1760**		Single-function MIL-STD-1760 interface module: supports single RT, BC, and Bus Monitor modes with an Internal Concurrent Monitor in RT and BC modes. Without error injection.
I*x*	**M4KDiscrete**		Discrete interface module: supports 20 bi-directional discretes with TTL (0 – 5V) or Avionic (0 – 32V) levels.
J*x*	**M4KSerial2**		Serial Interface module: supports two independent channels with RS485, RS422 or RS232 communication.
K*x*	**M4KSerial4**		Same as above - supports four independent channels.
L*x* (or M*x*)	**M4K1553Px-1760**		MIL-STD-1553 interface module: supports BC, multiple RTs, BC/ Concurrent-RT and BM modes with MIL-STD-1760 option. Supports an Internal Concurrent Monitor in RT and BC/RT modes.
O*x*	**M4KCAN2**		2 independent channels of CAN 2.0 B protocol with standard and extended message frames and message identifiers.
P*x*	**M4KCAN4**		Same as above with 4 independent channels.
Q*x*	**M4KCAN6**		Same as above with 6 independent channels.
R*x*	**M4KMMSI**		Mini Munitions Store Interface (MMSI) module. Supports RT, BC/Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 8 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and 1 composite monitor output.
T*x*	**M4K1553PxS**		Single-function MIL-STD-1553 interface module: supports single RT, BC, and Bus Monitor modes with an Internal Concurrent Monitor in RT and BC modes. Without error injection.
V*x*	**M4K1553PxM**		Monitor-only MIL-STD-1553 interface module.
		-E	Add this suffix for an extended temperature/ruggedized version of any module. The ruggedized version has an extended temperature range of -40º to +85º C.
		-001	Add this suffix for conformal coating.

Table 4-2 M4K Module Codes and Part Numbers (cont.)

More modules are in design. Check our website for the latest modules: www.mil-1553.com.

Note:

1. Use the **Module Part #** when ordering a module separately from the *EXC-4000P104plus*.
2. Use the **Module Codes** when ordering modules together with the *EXC-4000P104plus*.
3. The ***x*** in the **Module Code** denotes the number of consecutive modules of the same type on the board.

   Example: **F2** = 2 consecutive M4K1553Px modules

4. When ordering a board with a number of different protocol modules, the module codes must be in the following form:

   Example: EXC-4000P104P/A1F1I1F1T1

   The first module code in the part number is Module 0, the second is Module 1, and so on.

5. If one or more empty module locations are required in between other modules, insert an asterisk (*) followed by the number of empty locations, for example, *2.

   Example 1: EXC-4000P104P/B1*1O1F1

   This is an *EXC-4000P104plus* carrier board with:

   1 M4K429RT10 spread module at module location 0.
   Empty slot at module location 1.
   1 M4KCAN2 removable module at module location 2.
   1 M4K1553Px spread module at module location 3.
   Empty slot at module location 4.

   Example 2: EXC-4000P104P/*1F1

   This is an *EXC-4000P104plus* carrier board with:

   Empty slot at module location 0.
   1 M4K1553Px removable module at module location 1.
   Empty slots at module locations 2, 3 and 4.

6. Excalibur also offers a non-expandable version of the *EXC-4000P104plus* board. This board has only spread modules at module locations 0, 3 and 4. This board does not have the option of adding modules later. Add the **-L** suffix when ordering a non-expandable board.

   For non-expandable versions of the board, do not include asterisks for the empty removable module locations.

   Example 1: EXC-4000P104P/B1F1T1-L

   This is a non-expandable *EXC-4000P104plus* carrier board with:

   1 M4K429RT10 module at module location 0.
   Empty slot at module location 1.
   Empty slot at module location 2.
   1 M4K1553Px module at module location 3.
   1 M4K1553PxS module at module location 4.

Example 2: EXC-4000P104P/A1-L

This is a non-expandable *EXC-4000P104plus* carrier board with:

1 M4K429RT5 module at module location 0.
Empty slots at module locations 1, 2, 3 and 4.

October 2011, Rev B-3