EXC-2000PCI
&
EXC-2000PCIe

Test and Simulation Carrier Board for PCI Systems

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Note: The *EXC-2000PCIe* board will not work without the power cable connected. See 1.1 Installation on page 1-4.

1.1 Overview

The *EXC-2000PCI[e]* is a multiprotocol, PCI interface board for avionics test and simulation applications. Each board can hold up to 2 independent modules from the modules listed below:

M4K429RT*x*	ARINC 429 multi-channel interface module. This module supports either five or ten ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M4K708	ARINC 708 interface module. This module supports up to two ARINC 708/ 453 channels for the Weather Radar Display Databus. Each channel is selectable as transmit or receive and implements a 64K-word FIFO and supports polling and/or interrupt driven operation.
M4K717	ARINC 717 interface module. This module supports two ARINC 717 receive channels and two transmit channels.
M4KSerialPlus	Serial communications interface module. This module supports either two or four independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.
M4KDiscrete	Discrete I/O interface module. This module supports 20 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M4KCAN	CAN protocol interface module. This module supports either two, four or six independent channels of CAN 2.0B protocol with standard and extended message frames and message identifiers.
M4K825CAN	ARINC 825 interface module. The module supports up to ten ARINC 825 channels.

In addition Excalibur produces MIL-STD-1553, MMSI and H009 protocol modules for use with its *EXC-4000* family of carrier boards. More information about these and other Excalibur products is available on our website: www.mil-1553.com

All modules come with Windows drivers, including source code, mating connectors and plastic hoods.

1.1.1 Board Features

General Specifications

EXC-2000PCI[e]	Smaller than Half-size PCI or PCI Express Board (see Dimensions)
Supports up to 2 modules	
Protocols supported:	ARINC-429/575 (5 or 10 channels per module) ARINC 708/453 (2 ch. per module) ARINC 717 (2 ch. per module) Discrete I/O (20 ch. per module) Serial - RS485/RS422/RS232 (2 or 4 ch. per module) CAN (2, 4, or 6 ch. per module) ARINC 825 (CAN) (2, 4, 6 or 10 ch. per module)

Operating Environment

Temperature:	0° to 70°C standard temp. -40° to +85°C extended temp. (optional)
Humidity:	5% – 90% non-condensing

Physical Characteristics

	PCI Board	PCIe Board
Dimension	126.6mm (5”) x 106.7mm (4.2”)	120mm (4.72”) x 106.7mm (4.2”)
Weight	102g*	103g*

* without modules

Host Interface

PCI compliance:	Master/Target 8/16 bit
PCI Express compliance:	x1 lane PCIe v1.1 with incorporated DMA data transfer
Memory space occupied:	512 Kbytes
Interrupts:	INTA#
Power	Depends on configuration
MTBF	560,100 hours at 25°C, G_F, S217F

Software Support

C Drivers with source code
Mystic Windows software for 429 modules

For exact part numbers, see Chapter 4 **Ordering Information.**

1.1.2 Block Diagram

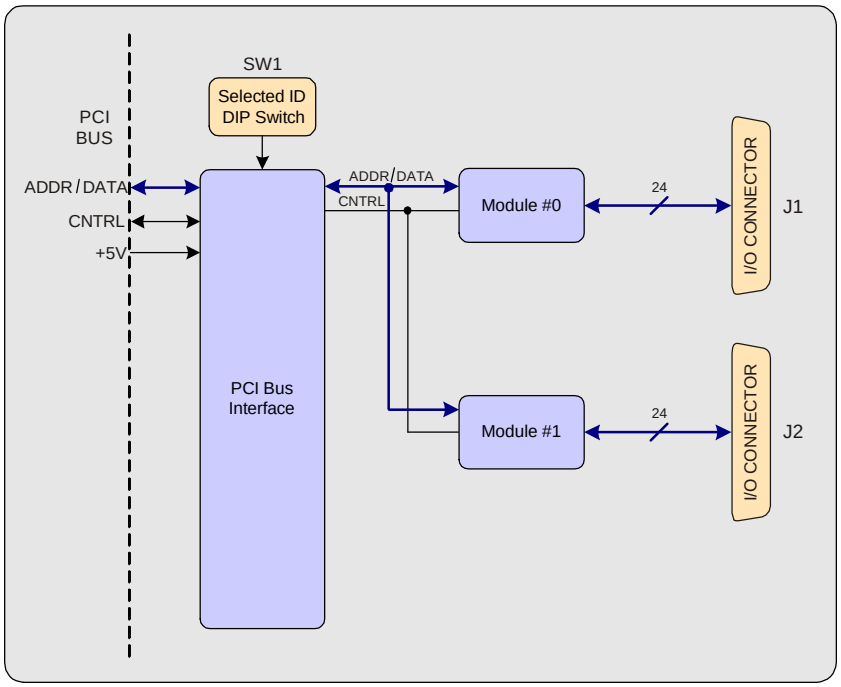

Figure 1-1 ***EXC-2000PCI*** **Block Diagram**

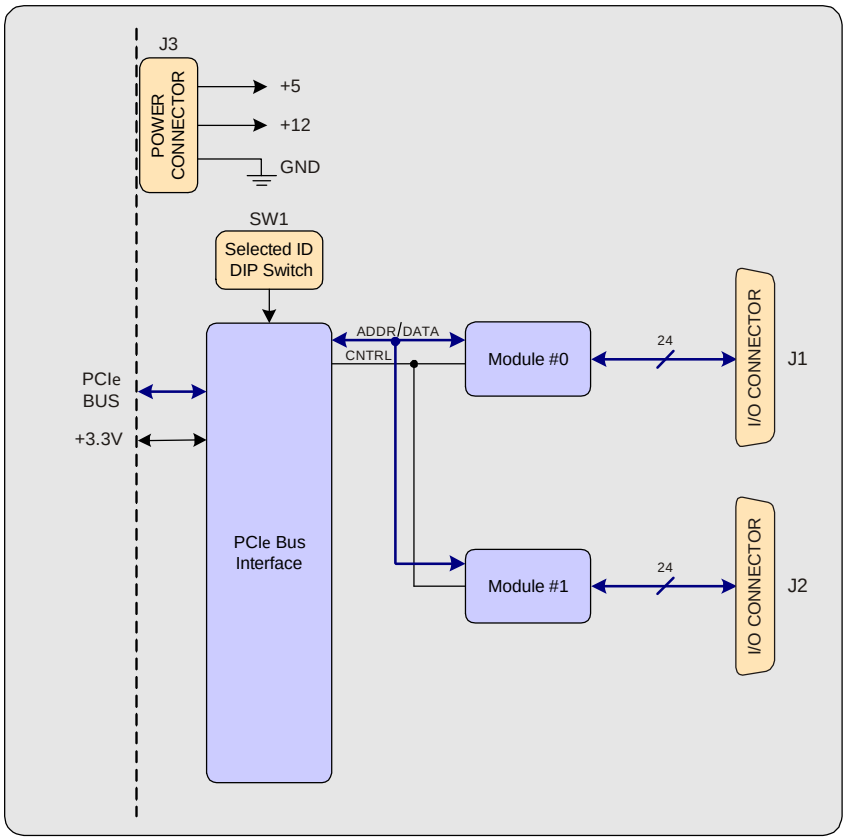

Figure 1-2 ***EXC-2000PCIe*** **Block Diagram**

1.1 Installation

For hardware and software installation instructions, see **Installation Instructions.pdf** in the root folder of the installation CD. When downloading new software from the Excalibur website, **Installation Instructions.pdf** is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see **Installation Instructions.pdf**. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.1 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the Technical Support page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the Contact Us page of our website. Before contacting Technical Support, please see Information Required for Technical Support.

2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:

2.1 Memory Structure

The *EXC-2000PCI* requests two memory blocks:

- The first memory block (Base 0) is 512 KB in size and contains the memory space for the modules on the board. For more information, see **2.8 Module Memory Space Map** on page 2-22.
- The second memory block (Base 1) is 64 bytes in size and contains the Global Registers. For more information, see **2.5 Global Registers Map** on page 2-12.

The *EXC-2000PCIe* requests two memory blocks:

- The first memory block (Base 0) is 512 KB in size and contains the memory space for the modules on the board. For more information, see **2.8 Module Memory Space Map** on page 2-22.
- The second memory block (Base 2) is 16 KB in size and contains the Global and DMA registers. For more information, see **2.5 Global Registers Map** on page 2-12 and **2.7 DMA Registers for PCI Express** on page 2-18.

2.2 PCI Configuration Space Header

The board includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The following figures show the PCI and PCIe Configuration Space Header:

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (not used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer (not used)				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2 (not used)				18 H
Base Address Register #1 – Global Registers				14 H
Base Address Register #0 Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1 PCI Configuration Space Header

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (not used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer (not used)				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2 – Global and DMA Registers				18 H
Base Address Register #1 (not used)				14 H
Base Address Register #0 – Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-2 PCI Express Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H

Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value: **PCI Board:** 4006 H
PCIe Board: E406 H

Size: 16 bits

The Device Identification register contains the board's device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	**PCI Board:** Always set to 1 **PCIe Board:** Always set to 0
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	**PCI Board:** Always set to 0 **PCIe Board:** Always set to 1
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the board does not use I/O space, the value of this register is ignored.

Table 2-1 PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	Not used
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 10 (slow timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 1
06	**Reserved**	
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
00-03	**Reserved**	

Table 2-2 PCI Status Register for PCI Boards

Bit	Bit Name	Description
15	Detected Parity Error	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	Signaled System Error	Not used
13	Received Master Abort	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	Received Target Abort	Not used
11	Signaled Target Abort	Not used
09-10	Device Select (DEVSEL#) Timing Status	Set to 00 (fast timing)
08	Data Parity Reported	Not used
07	Fast Back-to-Back Capable	Set to 0
06	UDF Supported	Set to 0
05	66MHz capable	Set to 0
04	Capability List enable	Set to 1
03	Interrupt Status	This bit is set when an interrupt is received.
00-02	Reserved	

Table 2-3 PCI Status Register for PCIe Boards

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the board.

2.3.6 Class Code Register (CLCD) Address: 09–-0B (H)

Power-up value: FF0000 H

Size: 24 bits

The Class code Register value indicates that the board does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) — Address: 0C (H)

Power-up value: **PCI Board:** 00 H
PCIe Board: 10 H

Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) — Address: 0D (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.9 Header Type Register (HDR) — Address: 0E (H)

Power-up value: 00 H

Size: 8 bits

The board is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) — Address: 0F (H)

Power-up value: 00 H

Size: 8 bits

The Built-In Self-Test register is not implemented in the board.

2.3.11 Base Address Registers (BADR)

Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

For PCI Boards: Two memory pages are required by the board: one for the Module Memory Space and one for the Global Registers.

Register	Offset	Size	Function
Base Address 0	10 H	512 K Byte	Module Memory Space
Base Address 1	14 H	64 Byte	Global registers

Table 2-4 Base Address Registers Definition for PCI Boards

For PCIe Boards: Two memory pages are required by the board: one for the Module Memory Space, one for the Global Registers and DMA Registers.

Register	Offset	Size	Function
Base Address 0	10 H	512 KB	Module Memory Space
Base Address 2	18 H	16 KB	Global and DMA registers

Table 2-5 Base Address Registers Definition for PCIe Boards

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

The following table describes the bits of the Base Address Register.

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 0 – memory is not prefetchable
01-02	Always 0 – memory may be mapped anywhere within the 32 bit memory space
00	Always 0 – indicates memory space

Table 2-6 Base Address Register for PCI Boards

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01-02	Always 2 – memory may be mapped anywhere within the 64 bit memory space
00	Always 0 – indicates memory space

Table 2-7 Base Address Register for PCIe Boards

2.3.12 Cardbus CIS Pointer — Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the board.

2.3.13 Subsystem ID — Address: 2C (H)

Power-up value: 0000 H

Size: 16 bits

2.3.14 Subvendor ID — Address: 2E (H)

Power-up value: 0000 H

Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM) — Address: 30 (H)

Power-up value: 00000000 H

Size: 32 bits

The Expansion ROM Space is not implemented on the board.

2.3.16 PCI Capabilities Pointer — Address: 34 (H)

Power-up value: 50 H

Size: 8 bits

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process.

2.3.17 Interrupt Line Register (INTLN) Address: 3C (H)

Power-up value: 00 H

Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either "unknown" or "no connection" for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) Address: 3D (H)

Power-up value: 01 H

Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) Address: 3E (H)

Power-up value: 00 H

Size: 8 bits

The Minimum Grant register is not implemented on the board.

2.3.20 Maximum Latency Register (MAXLAT) Address: 3F (H)

Power-up value: 00 H

Size: 8 bits

The Maximum Latency register is not implemented on the board.

2.4 Global and DMA Registers Memory Space Map

The Global and DMA Registers are mapped as follows.

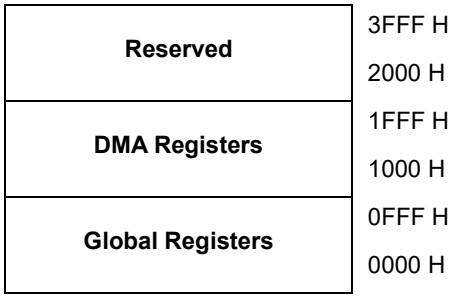

Figure 2-3 Global and DMA Registers Memory Space Map

2.5 Global Registers Map

The global registers reside in the second memory block.

Reserved	34 – 0FFF H
Board Type	32 H
2000PCI Family Identifier	30 H
Reserved	2A – 2E H
General Purpose Timer	28 H
Timer Control	26 H
Timer Preload	24 H
Timer Prescale	22 H
FPGA Revision	20 H
Reserved	14 – 1E H
Byte Swapping	12 H
Reserved	0C – 10 H
Module 1 Info	0A H
Module 0 Info	08 H
Interrupt Reset	06 H
Interrupt Status	04 H
Software Reset	02 H
Board ID	00 H

Figure 2-4 *EXC-2000PCI[e]* Global Registers Map

2.5.1 Board Identification Register

Address: 00 (H)
Length 16 bits

Read only The Board Identification register comprises the following identification items.

Bit	Description
04-15	**PCI Board:** Hard coded to the value 400 H **PCIe Board:** Hard coded to the value 4E0 H
00-03	Selected ID See **3.3.1 Selected ID DIP Switch [SW1] for Multiple Board Applications** on page 3-3.

Table 2-8 Board Identification Register

2.5.2 Software Reset Register

Address: 02 (H)
Length 16 bits

Write only The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the module's Time Tag counters.

Bit	Description	
05-15	Reserved – set to 0	
04	Global time tag reset	1 = reset all time tag counters 0 = no effect
02-03	Reserved – set to 0	
01	Module 1 reset	1 = reset module 0 = no effect
00	Module 0 reset	1 = reset module 0 = no effect

Table 2-9 Software Reset Register

2.5.3 Interrupt Status Register

Address: 04 (H)
Length 16 bits

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
05-15	Reserved – set to 0
04	1 = indicates that an interrupt was generated by the General Purpose Timer [See **2.6 Global Timer Registers** on page 2-16]
02-03	Reserved – set to 0
01	1 = indicates that module 1 is interrupting
00	1 = indicates that module 0 is interrupting

Table 2-10 Interrupt Status Register

Note: See also **2.7.7 DMA Interrupt Status Register** on page 2-21.

2.5.4 Interrupt Reset Register

Address: 06 (H)
Length 16 bits

Write only

The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
05-15	Reserved – set to 0
04	1 = Resets General Purpose Timer interrupt 0 = No effect
02-03	Reserved – set to 0
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Table 2-11 Interrupt Reset Register

Note: See also **2.7.7 DMA Interrupt Status Register** on page 2-21.

2.5.5 Module Info Registers

Address: 08, 0A (H)
Length 16 bits each

Read only

The Module Info Registers provide identification information for each of the modules.

Bit	Description	
12-15	Module ID	00 H = Module 0 Info register (at address 08 H) 01 H = Module 1 Info register (at address 0A H)
05-11	Reserved – set to 0	
00-04	Module type	02 H = *M4KSerial* 04 H = *M4K429RTx* module 07 H = *M4K708* module 08 H = *M4K825CAN* module (for *EXC-2000PCIe* only) 12 H = *M4KSerialPlus* module 17 H = *M4K717* module (for *EXC-2000PCIe* only) 0C H = *M4KCAN* module 0D H = *M4KDiscrete* module 1F H = no module installed

Table 2-12 Module Info Registers

2.5.6 Byte Swapping

Address: 12 (H)
Length 16 bits

Read/Write The Byte Swapping Register may be used to swap the high byte with the low byte of the Module Memory Space and the Global registers on the board. This may be useful on some host computers that byte-swap their memory.

Bit	Description	
00-15	A1A1	Enable byte swapping
	Any other value	Disable byte swapping **(Default)**

Table 2-13 Byte Swapping Register

2.5.7 FPGA Revision Register

Address: 20 (H)
Length 16 bits

Read only The FPGA Revision register contains the FPGA revision of the board. For example, for FPGA revision 1.5, the register would contain the value 0015 (H).

2.5.8 2000PCI Family Identifier Register

Address: 30 (H)
Length 16 bits

Read only The 2000PCI Family Identifier register is hard coded to value of 2000 (H).

2.5.9 Board Type Register

Address: 32 (H)
Length 16 bits

Read only The Board Type register comprises the following items.

Bit	Description
00-15	Hard coded to: **PCI Board:** 4006 H **PCIe Board:** E406 H

Board Type Register

2.6 Global Timer Registers

See **2.5 Global Registers Map** on page 2-12 for location of the registers on the memory map.

2.6.1 Timer Prescale Register

Address: 22 (H)
Bits 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Table 2-14 Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.6.2 Timer Preload Register

Address: 24 (H)
Bits 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.6.3 Timer Control Register

Address: 26 (H)
Bits 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose

Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1	Causes global reset of all installed modules
		0	No effect
02	Interrupt on count completed	1	Output an interrupt (see **2.5.3 Interrupt Status Register** on page 2-13)
		0	No effect
01	Reload mode	1	Reload mode
		0	Non-reload/One-shot mode
00	Start/Stop	1	Start
		0	Stop

Table 2-15 Timer Control Register

2.6.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only

The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

2.7 DMA Registers for PCI Express

Direct Memory Access (DMA) enables the board to access a module's memory space for reading and writing independently of the computer's CPU. This results in faster data transfer to and from the board, with much less CPU overhead than when not using DMA.

There are two DMA channels:

- **DMA0** – DMA channel 0 is used for DMA writes
- **DMA1** – DMA channel 1 is used for DMA reads

Reserved		1048 – 1FFF (H)
Repeat Code Register		1044 H
Base Address for DMA0 and DMA1 Transfers		1040 H
Reserved		1038 – 103C H
Reserved (Bits 2 – 31)	DMA Interrupt Status (Bits 0 – 1)	1034 H
Reserved		1020 – 1030 H
DMA1 Control		101C H
DMA1 Data Transfer Size		1018 H
DMA1 Address of Contiguous Host Memory – High 32 bits		1014 H
DMA1 Address of Contiguous Host Memory – Low 32 bits		1010 H
DMA0 Control		100C H
DMA0 Data Transfer Size		1008 H
DMA0 Address of Contiguous Host Memory – High 32 bits		1004 H
DMA0 Address of Contiguous Host Memory – Low 32 bits		1000 H

2.7.1 DMA0 Address of Contiguous Host Memory (Low and High)

Address: **1000 (H) (Low)**
1004 (H) (High)
Length **64 bits**

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data. Upon successful completion of a transfer, this register contains the following value: Start Address + Write Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.7.2 DMA0 Data Transfer Size

Address: 1008 (H)
Length 32 bits

This register contains the total amount of data (in bytes) to be written during a DMA write transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA write transfer, the value of this register should be 0.

2.7.3 DMA0 Control Register

Address: 100C (H)
Length 32 bits

This register contains information about, and controls, the DMA write data transfer.

Bit	Description	
12-13	Reserved – set to 0	
08-11	DMA channel state	These bits describe the state of the DMA write channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a module 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) The DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal module memory. 1100 – 1111 = (busy state) Reserved
04-07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00-01	Reserved – set to 0	

Table 2-16 DMA0 Control Register

2.7.4 DMA1 Address of Contiguous Host Memory

Address: 1010 (H) (Low)
1014 (H) (High)
Length 64 bits

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data.

Upon successful completion of a transfer, this register contains the following value: Start Address + Read Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.7.5 DMA1 Data Transfer Size

Address: 1018 (H)
Length 32 bits

This register contains the total amount of data (in bytes) to be read during a DMA read transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA read transfer, the value of this register should be 0.

2.7.6 DMA1 Control Register

Address: 101C (H)
Length 32 bits

This register contains information about, and controls, the DMA read data transfer.

Bit	Description	
12-13	Reserved – set to 0	
08-11	DMA channel state	These bits describe the state of the DMA read channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a module 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) The DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal module memory. 1100 – 1111 = (busy state) Reserved
04-07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00-01	Reserved – set to 0	

Table 2-17 DMA1 Control Register

2.7.7 DMA Interrupt Status Register

Address: 1034 (H)
Length 2 bits

Bit 0 of this register is set upon completion of a DMA transfer on DMA0 (DMA write). Bit 1 is set upon completion of a DMA transfer on DMA1 (DMA read). To clear either bit, write a 1 to the corresponding location.

Note: The two bits of the DMA Interrupt Status Register work together with the five bits of the Global Interrupt Status Register. When any of these seven bits are set, an interrupt is generated. To locate the source of an interrupt to the host, both of these registers need to be read.

In order to reset an interrupt, you must reset the appropriate bits of **both** the DMA Interrupt Status Register **and** the Global Interrupt Reset Register. See **2.5.3 Interrupt Status Register** on page 2-13.

2.7.8 Base Address for DMA0 and DMA1 Transfers

Address: 1040 (H)
Length 32 bits

This register contains the start address of the current DMA transfer (read or write transfer). The base must be written to this register by the user.

2.7.9 Repeat Code Register

Address: 1044 (H)
Length 32 bits

This register determines the type of DMA reads and writes done by the board. When bits 00–03 are set to 0, the board performs standard DMA reads and writes. When bits 00–03 set to 1, 2, 4 or 8, the board performs FIFO reads/writes of either 1, 2, 4 or 8, bytes.

Bit	Description	
04-31	Reserved – set to 0	
00-03	Repeat Code	0000 = Start DMA transfer 0001 = 1-byte FIFO reads/writes 0010 = 2-byte FIFO reads/writes 0100 = 4-byte FIFO reads/writes 1000 = 8-byte FIFO reads/writes

Table 2-18 Repeat Code Register

2.8 Module Memory Space Map

The Module Memory Space map resides in the first memory block. Each module is allocated a space of 128 KB which is mapped as shown in **Figure 2-5 Module Memory Space Map**. (See **Chapter 4 Ordering Information** for information on the available modules for this carrier board.)

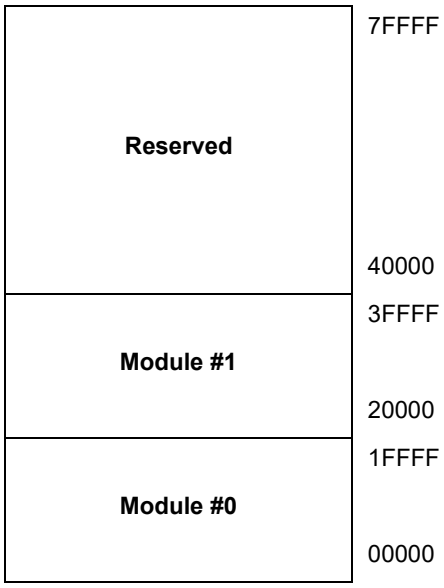

Figure 2-5 Module Memory Space Map

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-2000PCI[e]* carrier board.

3.1 Board Layout

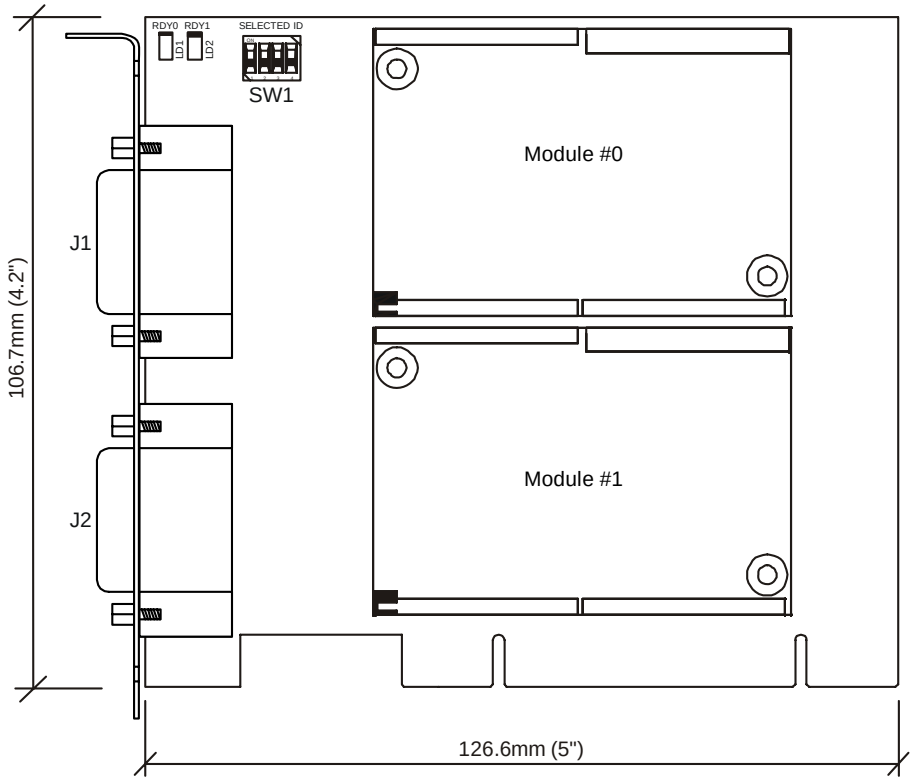

Figure 3-1 ***EXC-2000PCI*** **Board Layout**

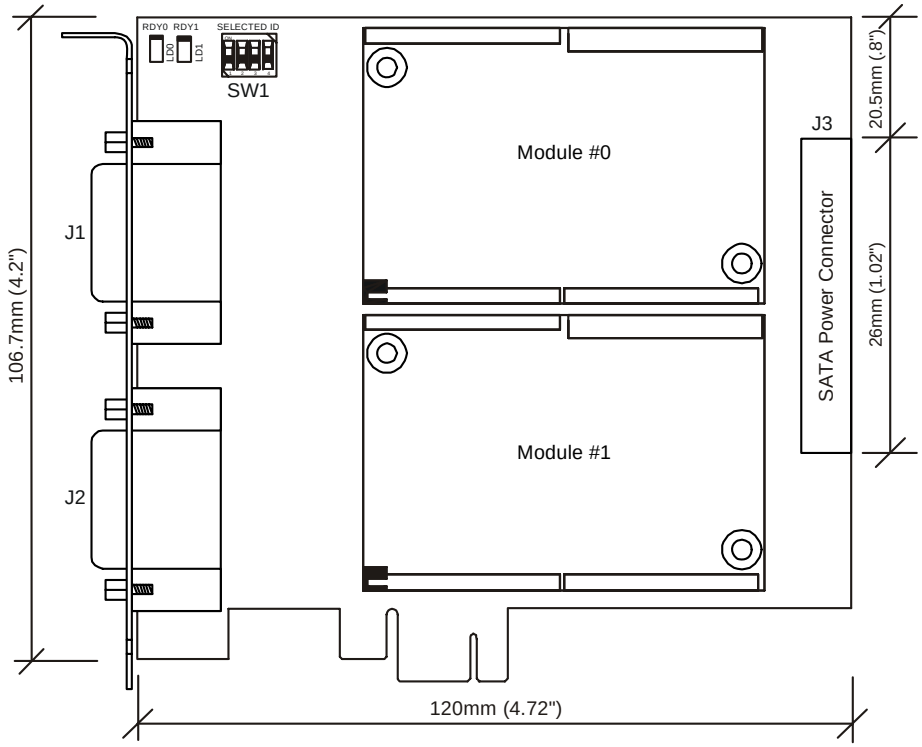

Figure 3-2 ***EXC-2000PCIe*** **Board Layout**

3.2 LED Indicators

The *EXC-2000PCI[e]* contains two LEDs.

PCIe LED	PCI LED	Name	Indication
LD0	**LD1**	RDY0	Module 0 Ready
LD1	**LD2**	RDY1	Module 1 Ready

Table 3-1 LED Indicators

3.3 DIP Switches

- The *EXC-2000PCI[e]* contains one DIP switch (SW1).

3.3.1 Selected ID DIP Switch [SW1] for Multiple Board Applications

When using more than one board in the same computer, it is necessary to set a unique **Selected ID** for each board, using the SW1 DIP switch. After setting the Selected ID, use the ExcConfig utility to associate the Selected ID with a **device number**. *Excalibur Software Tools* use the device number to identify the board. Note that in the ExcConfig utility, the Selected ID is called the Unique ID.

This DIP switch has four contacts and represents a four bit value, of which position #1 is the most significant bit. When a specific contact in the DIP switch is:

- **OFF** a value of "1" is set for that bit
- **ON** a value of "0" is set for that bit

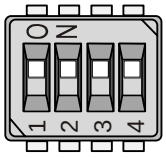

Figure 3-3 DIP Switch SW1 with All Contacts Set to ON (Selected ID#0)

The following table shows the required contact positions to represent various Selected ID values.

For Selected ID #	Contact 1 (MSB)	Contact 2	Contact 3	Contact 4 (LSB)
0	ON (0)	ON (0)	ON (0)	ON (0)
1	ON (0)	ON (0)	ON (0)	OFF (1)
2	ON (0)	ON (0)	OFF (1)	ON (0)
3	ON (0)	ON (0)	OFF (1)	OFF (1)
•				
•				
•				
15	OFF (1)	OFF (1)	OFF (1)	OFF (1)

Table 3-2 Selected ID Values

3.4 Connectors

3.4.1 *EXC-2000PCI* Connectors

The *EXC-2000PCI* contains the following connectors:

1. Two high-density, female HDB-26 pin connectors [J1 and J2] contain all the modules I/O signals [P/N Amphenol G17BH-2600-132 or equivalent]. See section **3.4.3 Communications I/O Connector [J1] and [J2],** page 3-5.

   Standard high-density, male HDB-26 pin mating connectors and plastic hoods are provided.

2. A PCI bus edge connector passes all of the PCI signals, see section **3.4.4 PCI Bus Edge Connector Pinout** on page 3-13.

3.4.2 *EXC-2000PCIe* Connectors

The *EXC-2000PCIe* contains the following connectors:

1. Two high-density, female HDB-26 pin connectors [J1 and J2] contain all the modules I/O signals [P/N Amphenol G17BH-2600-132 or equivalent]. See section **3.4.3 Communications I/O Connector [J1] and [J2],** page 3-5.

   Standard high-density, male HDB-26 pin mating connectors and plastic hoods are provided.

2. A PCI Express bus edge connector passes all of the PCI Express signals, see section **3.4.5 PCI Express Bus Edge Connector Pinout** on page 3-14.

3. A standard, full SATA, right-angle, male 15+7-pin connector [J3] provides the required power for all the modules, but not for the PCIe interface. Use only the power section of this connector. The signal pins are not connected to the board [P/N Amphenol SATA-001-0225-3]. See section **3.4.6 SATA Connector for PCI Express for Power Only [J3]** on page 3-15.

   The mating connector is a standard SATA 15-pin female power connector found in most computers. This is one of the standard power connectors attached to the computer's power supply via power cables.

3.4.3 Communications I/O Connector [J1] and [J2]

Two high-density, female HDB-26 pin connectors [J1 and J2] contain all the modules I/O signals. J1 passes the I/O signals for Module 0 and J2 passes the I/O signals for Module 1.

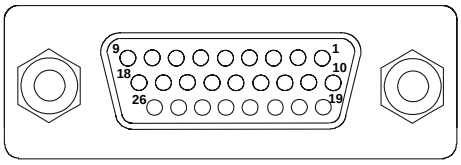

Figure 3-4 High-density HDB-26 Pin Female Connector – Front View

The pinouts of the J1 and J2 connectors vary depending on the modules installed on the board. The following tables list the pinouts per module.

3.4.3.1 J1/J2 Connector Pinouts for *M4K429RTx* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0L	ARINC 429 Channel 0 low connection
3	CH0H	ARINC 429 Channel 0 high connection
4	CH1L	ARINC 429 Channel 1 low connection
5	CH1H	ARINC 429 Channel 1 high connection
6	CH2L	ARINC 429 Channel 2 low connection
7	CH2H	ARINC 429 Channel 2 high connection
8	CH3L	ARINC 429 Channel 3 low connection
9	CH3H	ARINC 429 Channel 3 high connection
10	CH4L	ARINC 429 Channel 4 low connection
11	CH4H	ARINC 429 Channel 4 high connection
12	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH5L	ARINC 429 Channel 5 low connection
14	CH5H	ARINC 429 Channel 5 high connection
15	CH6L	ARINC 429 Channel 6 low connection
16	CH6H	ARINC 429 Channel 6 high connection
17	CH7L	ARINC 429 Channel 7 low connection
18	CH7H	ARINC 429 Channel 7 high connection
19	CH8L	ARINC 429 Channel 8 low connection
20	CH8H	ARINC 429 Channel 8 high connection
21	CH9L	ARINC 429 Channel 9 low connection
22	CH9H	ARINC 429 Channel 9 high connection
23	OUTRIGn	This low active output provides trigger pulses of approximately 400 nsec. width and is activated under software control upon the same conditions as interrupts. See Interrupt/ Trigger Mask Registers. This output is an open-collector with 330-ohm pull-up resistor.
24	GND	Provides ground reference for the OUTRIGn output.
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-3 J1/J2 Connector Pinouts for *M4K429RTx* Modules

3.4.3.2 J1/J2 Connector Pinouts for *M4K708* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	BUS0L	Channel 0 low connection
3	BUS0H	Channel 0 high connection
4 – 9	N/C	Not connected
10	BUS1L	Channel 1 low connection
11	BUS1H	Channel 1 high connection
12	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13 – 18	N/C	Not connected
19 – 22	Reserved	Do not use this pin.
23	OUTRIGn	Output trigger low active output. Provides trigger pulses of approximately 500 nsec. width and is activated upon the same conditions as interrupts. See Channel Output Trigger Mask Register in the *M4K708 Module User's Manual*. This output is an open-collector type pulled up with a 330-Ohm resistor to 5V.
24	GND	Provides ground reference for the OUTRIGn output.
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-4 J1/J2 Connector Pinouts for *M4K708* Modules

3.4.3.3 J1/J2 Connector Pinouts for *M4K717* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0TxL	Channel 0 Tx low connection
3	CH0TxH	Channel 0 Tx high connection
4	CH0RxL	Channel 0 Rx low connection
5	CH0RxH	Channel 0 Rx high connection
6	N/C	Not connected
7	N/C	Not connected
8	N/C	Not connected
9	N/C	Not connected
10	N/C	Not connected
11	N/C	Not connected
12	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH1TxL	Channel 1 Tx low connection
14	CH1TxH	Channel 1 Tx high connection
15	CH1RxL	Channel 1 Rx low connection
16	CH1RxH	Channel 1 Rx high connection
17	N/C	Not connected
18	N/C	Not connected
19	N/C	Not connected
20	N/C	Not connected
21	N/C	Not connected
22	N/C	Not connected
23	OUTRIGn	Trigger Output. This low active LVTTL open-collector output with a 330-Ohm pull-up resister provides trigger pulses of approximately 110 nsec. width and is activated under software control upon the same conditions as interrupts. See **Trigger Mask Register**.
24	GND	Provides ground reference for the OUTRIGn output.
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-5 J1/J2 Connector Pinouts for M4K717 Modules

3.4.3.4 J1/J2 Connector Pinouts for *M4KSerialPlus* Modules

J1/J2 Pin #	Signal Description		
	RS-232	**RS-485**	**RS-422**
1	Do not use this pin.		
2	N/C	Channel 0 high connection	Channel 0 Transmit high connection
3	Channel 0 Transmit connection	Channel 0 low connection	Channel 0 Transmit low connection
4	Channel 0 Receive connection	N/C	Channel 0 Receive high connection
5	N/C	N/C	Channel 0 Receive low connection
6	Provides ground reference	N/C	N/C
7	Do not use this pin.		
8	N/C	Channel 1 high connection	Channel 1 Transmit high connection
9	Channel 1 Transmit connection	Channel 1 low connection	Channel 1 Transmit low connection
10	Channel 1 Receive connection	N/C	Channel 1 Receive high connection
11	N/C	N/C	Channel 1 Receive low connection
12	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.		
13	N/C	Channel 2 high connection	Channel 2 Transmit high connection
14	Channel 2 Transmit connection	Channel 2 low connection	Channel 2 Transmit low connection
15	Channel 2 Receive connection	N/C	Channel 2 Receive high connection
16	N/C	N/C	Channel 2 Receive low connection
17	Provides ground reference	N/C	N/C
18	Do not use this pin.		
19	N/C	Channel 3 high connection	Channel 3 Transmit high connection
20	Channel 3 Transmit connection	Channel 3 low connection	Channel 3 Transmit low connection
21	Channel 3 Receive connection	N/C	Channel 3 Receive high connection
22	N/C	N/C	Channel 3 Receive low connection
23	Do not use this pin.		
24	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.		
25	Not connected – Reserved		
26	Not connected – Reserved		

Table 3-6 J1/J2 Connector Pinouts for *M4KSerialPlus* Modules

3.4.3.5 J1/J2 Connector Pinouts for *M4KDiscrete* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	IO0	Discrete 0
2	IO1	Discrete 1
3	IO2	Discrete 2
4	IO3	Discrete 3
5	IO4	Discrete 4
6	IO5	Discrete 5
7	IO6	Discrete 6
8	GND	Provides ground reference for input and output Discretes
9	IO7	Discrete 7
10	IO8	Discrete 8
11	EXT_TRIG	TTL Active low External trigger (pulse width approx. 150 nS)
12	SHIELD	Provides the input and output Discretes with shield connections. This signal is connected to the case of the computer.
13	IO9	Discrete 9
14	IO10	Discrete 10
15	IO11	Discrete 11
16	IO12	Discrete 12
17	IO13	Discrete 13
18	IO14	Discrete 14
19	IO15	Discrete 15
20	IO16	Discrete 16
21	GND	Provides ground reference for input and output Discretes
22	IO17	Discrete 17
23	IO18	Discrete 18
24	IO19	Discrete 19
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-7 J1/J2 Connector Pinouts for *M4KDiscrete* Modules

3.4.3.6 J1/J2 Connector Pinouts for *M4KCAN* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
2	CAN0H	Channel 0 high connection
3	CAN0L	Channel 0 low connection
4	CAN1H	Channel 1 high connection
5	CAN1L	Channel 1 low connection
6	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
7	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
8	CAN2H	Channel 2 high connection
9	CAN2L	Channel 2 low connection
10	CAN3H	Channel 3 high connection
11	CAN3L	Channel 3 low connection
12	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
13	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
	N/C	Not connected
14	CAN4H	Channel 4 high connection
15	CAN4L	Channel 4 low connection
16	CAN5H	Channel 5 high connection
17	CAN5L	Channel 5 low connection
18	SHIELD	Provided for CAN cables shield connection. This signal is connected to the case of the computer
19	Reserved	Do not use this pin.
20	Reserved	Do not use this pin.
21	GND	Provides ground reference
22	N/C	Not connected
23	N/C	Not connected
24	N/C	Not connected
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-8 J1/J2 Connector Pinouts for *M4KCAN* Modules

3.4.3.7 J1/J2 Connector Pinouts for *M4K825CAN* Modules

J1/J2 Pin #	Signal Name	Signal Description
1	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0L	Channel 0 low connection
3	CH0H	Channel 0 high connection
4	CH1L	Channel 1 low connection
5	CH1H	Channel 1 high connection
6	CH2L	Channel 2 low connection
7	CH2H	Channel 2 high connection
8	CH3L	Channel 3 low connection
9	CH3H	Channel 3 high connection
10	CH4L	Channel 4 low connection
11	CH4H	Channel 4 high connection
12	SHIELD	Provided for the cable's shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH5L	Channel 5 low connection
14	CH5H	Channel 5 high connection
15	CH6L	Channel 6 low connection
16	CH6H	Channel 6 high connection
17	CH7L	Channel 7 low connection
18	CH7H	Channel 7 high connection
19	CH8L	Channel 8 low connection
20	CH8H	Channel 8 high connection
21	CH9L	Channel 9 low connection
22	CH9H	Channel 9 high connection
23	OUTRIGn	Trigger Output. This low active LVTTL open-collector output with a 330-Ohm pull-up resister provides trigger pulses of approximately 110 nsec. width and is activated under software control upon the same conditions as interrupts. See **Trigger Mask Register**.
24	GND	Provides ground reference
25	N/C	Not connected – Reserved
26	N/C	Not connected – Reserved

Table 3-9 J1/J2 Connector Pinouts for *M4K825CAN* Modules

3.4.4 PCI Bus Edge Connector Pinout

Pin	PCI Names	Board Signal Names
B1	-12V	-12V
B2	TCK	
B3	GROUND	GND
B4	TDO	
B5	+5V	VCC
B6	+5V	VCC
B7	INTB#	
B8	INTD#	
B9	PRSNT1#	GND
B10	RESERVED	
B11	PRSNT2#	
B12 B13	CONNECTOR KEY	
B14	RESERVED	
B15	GROUND	GND
B16	CLK	CLK
B17	GROUND	GND
B18	REQ#	Arden
B19	+5V (I/O)	
B20	AD[31]	AD31
B21	AD[29]	AD29
B22	GROUND	GND
B23	AD[27]	AD27
B24	AD[25]	AD25
B25	+3.3V	+3.3V
B26	C/BE[3]#	C_BE3n
B27	AD[23]	AD23
B28	GROUND	GND
B29	AD[21]	AD21
B30	AD[19]	AD19
B31	+3.3V	+3.3V
B32	AD[17]	AD17
B33	C/BE[2]#	C_BE2n
B34	GROUND	GND
B35	IRDY#	Arden
B36	+3.3V	+3.3V
B37	DEVSEL#	Devising
B38	GROUND	GND
B39	LOCK#	Locking
B40	PERR#	Preen
B41	+3.3V	+3.3V
B42	SERR#	Siren
B43	+3.3v	+3.3V
B44	C/BE[1]#	C_BE1n
B45	AD[14]	AD14
B46	GROUND	GND
B47	AD[12]	AD12
B48	AD[10]	AD10
B49	GROUND	GND
B50 B51	CONNECTOR KEY	
B52	AD[08]	AD8
B53	AD[07]	AD7
B54	+3.3V	+3.3V
B55	AD[05]	AD5
B56	AD[03]	AD3
B57	GROUND	GND
B58	AD[01]	AD1
B59	+5V (I/O)	
B60	ACK64#	
B61	+5V	VCC
B62	+5V	VCC

Pin	PCI Names	Board Signal Names
A1	TRST#	
A2	+12V	+12V
A3	TMS	
A4	TDI	
A5	+5V	VCC
A6	INTA#	INTAn
A7	INTC#	
A8	+5V	VCC
A9	RESERVED	
A10	+5V	
A11	RESERVED	
A12 A13	CONNECTOR KEY	
A14	RESERVED	
A15	RST#	RSTn
A16	+5V	
A17	GNT#	GNTn
A18	GROUND	GND
A19	RESERVED	
A20	AD[30]	AD30
A21	+3.3V	+3.3V
A22	AD[28]	AD28
A23	AD[26]	AD26
A24	GROUND	GND
A25	AD[24]	AD24
A26	IDSEL	IDSEL
A27	+3.3V	+3.3V
A28	AD[22]	AD22
A29	AD[20]	AD20
A30	GROUND	GND
A31	AD[18]	AD18
A32	AD[16]	AD16
A33	+3.3V	+3.3V
A34	FRAME#	Freeman
A35	GROUND	GND
A36	TRDY#	Trodden
A37	GROUND	GND
A38	STOP#	Stop
A39	+3.3V	+3.3V
A40	SDONE	
A41	SBO#	
A42	GROUND	GND
A43	PAR	PAR
A44	AD[15]	AD15
A45	+3.3V	+3.3V
A46	AD[13]	AD13
A47	AD[11]	AD11
A48	GROUND	GND
A49	AD[09]	AD9
A50 A51	CONNECTOR KEY	
A52	C/BE[0]#	C_BE0n
A53	+3.3V	+3.3V
A54	AD[06]	AD6
A55	AD[04]	AD4
A56	GROUND	GND
A57	AD[02]	AD2
A58	AD[00]	AD0
A59	+5V	
A60	REQ64#	
A61	+5V	VCC
A62	+5V	VCC

Table 3-10PCI Bus Edge Connector Pinout

3.4.5 PCI Express Bus Edge Connector Pinout

	Side B Connector		Side A Connector	
Pin	**Signal Name**	**Description**	**Signal Name**	**Description**
1	+12V	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12V	+12 volt power	+12V	+12 volt power
3	RSVD	Reserved	+12V	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3V	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3V	+3.3 volt power
10	3.3Vaux	3.3 volt auxiliary power	+3.3V	+3.3 volt power
11	WAKE#	Link reactivation	PWRGD	Power good
MECHANICAL KEY				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock, differential pair
14	HSOp	Transmitter lane, differential pair	REFCLK-	
15	HSOn		GND	Ground
16	GND	Ground	HSIp	Receiver lane, differential pair
17	PRSNT#2	Hot plug detect	HSIn	
18	GND	Ground	GND	Ground

Table 3-11 PCI Express Bus Edge Connector Pinout

3.4.6 SATA Connector for PCI Express for Power Only [J3]

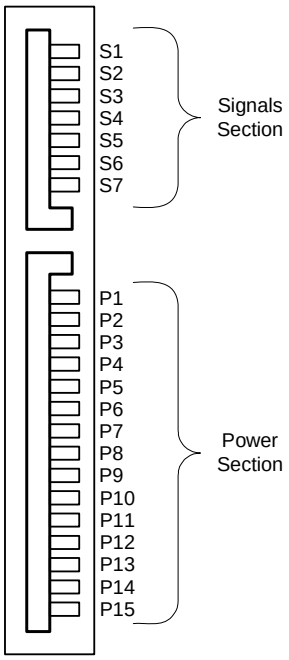

Figure 3-5 15+7-Pin Male SATA Connector [J3] – Front View

Pin	Signal
S1	Not connected
S2	Not connected
S3	Not connected
S4	Not connected
S5	Not connected
S6	Not connected
S7	Not connected
P1	Not connected
P2	Not connected
P3	Not connected
P4	GND
P5	GND
P6	GND
P7	+5V
P8	+5V
P9	+5V
P10	GND
P11	Not connected
P12	GND
P13	+12V
P14	+12V
P15	+12V

Table 3-12 15+7-Pin Male SATA Connector Pin-outs [J3]

Note: The *EXC-2000PCIe* board will not work without the power cable connected.

The power section of this connector mates with the standard PC SATA power supply cable. See section **1.1 Installation** on page 1-4. (The signal pins are not connected on the board.)

3.5 Power Requirements

The *EXC-2000PCI[e]* maximum power requirements, without any modules installed, are:

	+3.3V	+5V
EXC-2000PCI	N/A	100mA
EXC-2000PCIe	330mA	N/A

***EXC-2000PCI[e]* Power Requirements**

When using an *EXC-2000PCI* board, the power for the board and its modules is drawn from PCI bus edge connector.

When using an *EXC-2000PCIe* board, the power for the board is drawn from the PCI Express bus edge connector and the power for its modules is drawn from the power connector [J3]. See **3.4.6 SATA Connector for PCI Express for Power Only [J3]** on page 3-15.

The final power requirements will depend on how many and which modules are installed. To calculate the exact carrier board power requirements, see the specific module's *User's Manual*.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering an *EXC-2000PCI[e]* carrier board.

Basic Part #	Option	Description
EXC-2000PCI/*xx*		Multiprotocol carrier board for PCI compatible systems with up to two modules.
EXC-2000PCIe/*xx*		Multiprotocol carrier board for PCI Express (PCIe) compatible systems with up to two modules.
		Replace '***xx***' with the module codes of the modules you want. See Table 4-2.
		When ordering the board without modules, leave the '***xx***' in the part number. When ordering a module separate from a carrier board, use the module part # in Table 4-2. See the user's manual of the module for complete ordering information.
	-E	Add this suffix for extended temperature/ruggedized version. All the modules come with a ruggedized, extended temperature option (-40° to + 85°C).
	-001	Add this suffix for conformal coating.

Table 4-1 Ordering Information

Note: Adapter cables and External Loopback test connectors are available for most configurations. Contact Excalibur Sales for more information.

Module Code (for Ordering with Carrier Board)	Module Part # (for Ordering Separately)	Description
A*x*	**M4K429RT5**	ARINC 429 interface module: supports up to five channels.
B*x*	**M4K429RT10**	ARINC 429 interface module: supports up to ten channels.
C*x*	**M4K708**	The module supports two ARINC 708/453 channels, each one selectable as either transmit or receive.
I*x*	**M4KDiscrete**	Discrete interface module: supports 20 bi-directional Discretes with TTL (0 – 5V) or Avionic (0 – 32V) levels.
JJ*x*	**M4KSerialPlus2**	Serial interface module – supports two independent channels with RS485, RS422 or RS232 communication.
KK*x*	**M4KSerialPlus4**	Same as above with four independent channels.
N*x*	**M4K717**	ARINC 717 interface module – supports two ARINC 717 receive channels and two transmit channels.
O*x*	**M4KCAN2**	2 independent channels of CAN 2.0 B protocol with standard and extended message frames and message identifiers.
P*x*	**M4KCAN4**	Same as above with 4 independent channels.
Q*x*	**M4KCAN6**	Same as above with 6 independent channels.

Table 4-2 M4K Module Codes and Part Numbers

Module Code (for Ordering with Carrier Board)	Module Part # (for Ordering Separately)	Description
SA*x*	**M4K825CAN2**	ARINC 825 interface module – supports two ARINC 825 channels.
SB*x*	**M4K825CAN4**	ARINC 825 interface module – supports four ARINC 825 channels.
SC*x*	**M4K825CAN6**	ARINC 825 interface module – supports six ARINC 825 channels.
SD*x*	**M4K825CAN10**	ARINC 825 interface module – supports 10 ARINC 825 channels.
Options	Add **-E** at the end of the part number for an extended temperature/ ruggedized version of any module. The ruggedized version has an extended temperature range of -40º to +85º C.	
	Add **-001** at the end of the part number for conformal coating.	

Table 4-2 M4K Module Codes and Part Numbers (Continued)

More modules are in design. Check www.mil-1553.com for the latest modules.

Note:

- Use the Module part# if ordering separately from the *EXC-2000PCI[e]*.
- The ***x*** following the module code denotes the number of modules per board.

  Example: B2 = 2 × ARINC 429 M4K429RT10 modules.

- The *EXC-2000PCI[e]* does not support MIL-STD-1553, MMSI or H009 protocols.
- Customers who wish to use MIL-STD-1553, MMSI or H009 protocols should purchase the *EXC-4000PCIHC* carrier board.

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