M4K1553Px

MIL-STD-1553
Test and Simulation Module for the EXC-4000 Family of Carrier Boards

User's Manual

EXCALIBUR SYSTEMS

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Table of Contents

4 Bus Monitor Operation

Figures

Tables

1 Introduction

Chapter 1 provides an overview of the *M4K1553Px* avionics communication module. The following topics are covered:

1.1 Overview

The *M4K1553Px* is an intelligent, multifunction MIL-STD-1553 interface module for the multimode, multiprotocol, Excalibur 4000 family of carrier boards. The *M4K1553Px* provides a complete solution for developing and testing 1553 interfaces and performing system simulation of the MIL-STD-1553 bus. The module handles all standard variations of the MIL-STD-1553 protocol. Each module of the *M4K1553Px* contains 64K bytes of dual-port RAM for Data Blocks, Control registers, and Look-up Tables. All Data Blocks and Control registers are memory mapped, and may be accessed in real time.

Each of the independent dual redundant *M4K1553Px* modules may be programmed to operate in one of three modes of operation: Remote Terminal, BC/Concurrent-RT, and Bus Monitor. In addition, one module can be programmed to operate as Concurrent monitor for another module. See **4.13.3 Internal Monitor Connect Register** on page 4-25.

The standard multifunction module (*M4K1553Px*) supports up to 32 RTs in RT and BC/Concurrent-RT modes.

The *M4K1553PxS* is a single function version of the module, that simulates only one RT and does not support BC/Concurrent-RT mode. For more details, see **1.1.4 Single Function Option (PxS)** on page 1-5.

The *M4K1553PxM* is a monitor-only version of the module.

The *M4K1553Px-LB* provides an Onboard Loopback option for External Loopback testing without the need for an External Loopback cable. See **3.13.4 Loopback Relay Select Register** on page 3-20.

The *-E* option (*M4K1553Px-E*) is an extended temperature (-40° to +85°C) version of the module.

The module comes complete with Windows software, a C-driver software library including source code, and 1553 mating connectors with plastic hoods.

Important This manual applies to module Rev G or later. For earlier module revisions, refer to the appropriate *User's Manual*.

Note: The *M4K1553Px* module can be mounted on the following Excalibur carrier boards:

- *EXC-4000PCIe*
- *EXC-4000[c]PCI*
- *EXC-4000VME*
- *EXC-4000VXI*
- *EXC-4000P104plus*
- *EXC-4500ccVPX*
- *EXC-664PCIe*
- *EXC-ETHPCIe*

1.1.1 Module Features

Independent 1553 dual-redundant module

Real-time operation

Operates as RT, BC/Concurrent-RT or Triggerable Bus Monitor

Concurrent monitor in RT and BC/RT modes

Multiple protocol capability (i.e. 1553A/B, F-16)

Multiple-RT simulation (up to 32 Remote Terminals)

Extended Temperature range available – -40º to +85ºC

Programmable broadcast mode

Multi-mode triggerable Monitor

Extensive interrupt features

Error injection capability:
- Word Count (+/-3 words)
- Bit Count (+/-3 bits)
- Incorrect sync
- Incorrect RT address
- Incorrect parity
- Non-contiguous data

Service Request Processing

MIL-STD-1760 Option (-1760)

Checksum error detection

Checksum error injection

Header Words

Single Function Option (*PxS*)

Operates as a single RT, BC or Triggerable Bus Monitor (no Concurrent RT)

RT address can be set via module connector

No error injection

Fixed amplitude

Monitor-only Option (*PxM*)

Operates as Bus Monitor only

Onboard Loopback Option (-LB)

Makes a loopback connection without the need for an External Loopback cable

Allows a full onboard built-in test

See **Chapter 8: Ordering Information**, for the exact part numbers.

Examples of user selectable parameters are:

- The user can select whether an RT will return a Status Word in the event a message containing a Data Word error is received by the RT.
- Selectable broadcast mode
- Variable response time
- Select Mode Code subaddress (00000, 11111, or both)
- 1553A RT timing
- Each bit in the 1553 Status Word can be defined by the user

The *M4K1553Px* has three modes of operation:

- Multiple Remote Terminal (RT) mode (up to 32 RTs)
- BC with Concurrent RT operation (up to 32 RTs)
- Triggerable Monitor mode

1.1.2 Block Diagram

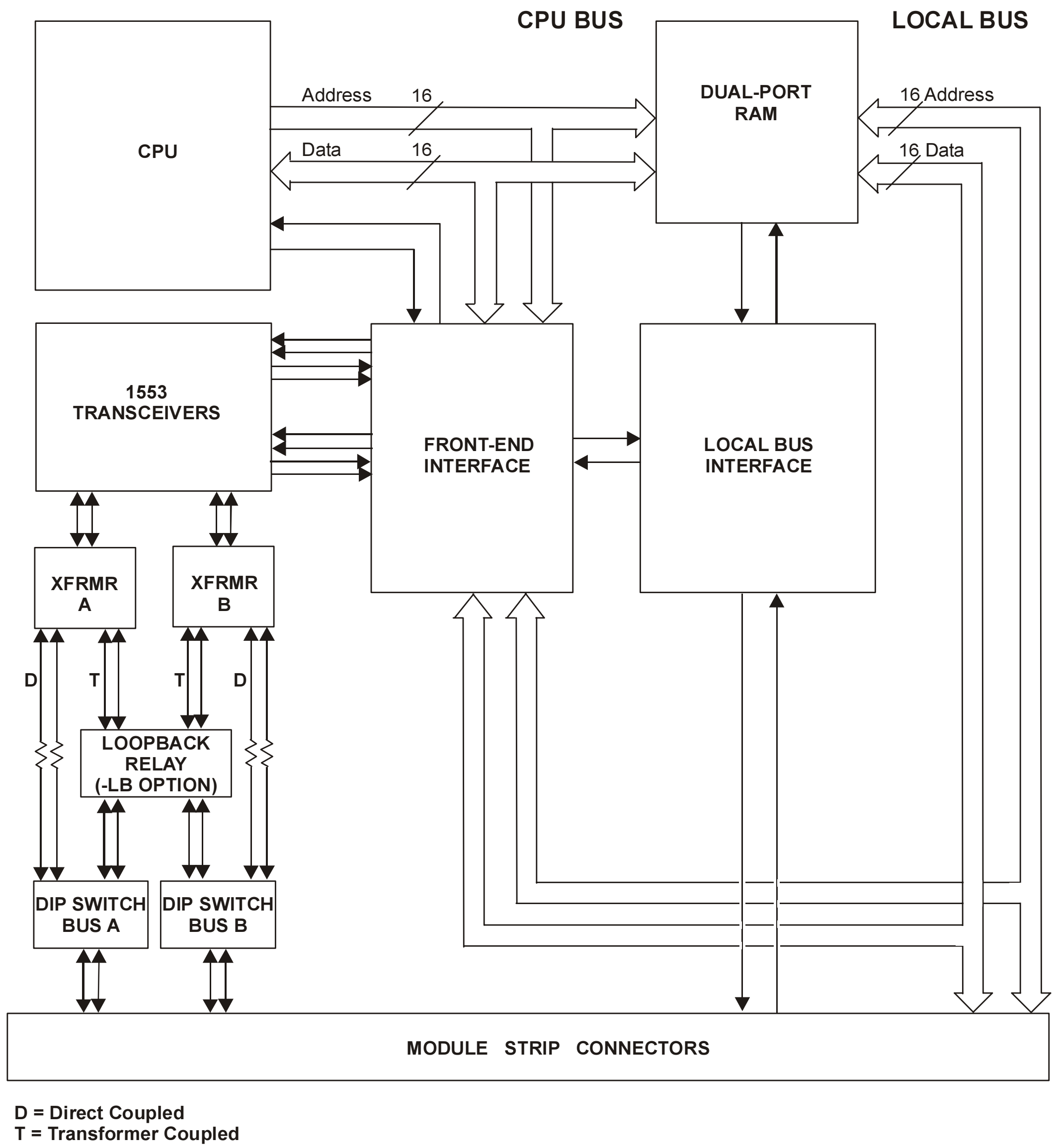


Figure 1-1 ***M4K1553Px*** **Block Diagram**

1.1.3 1760 Option

MIL-STD-1760 implements an enhanced MIL-STD-1553 digital interface for the transfer of digital messages to the remote terminal. The enhancements include additional error detection in the form of checksum. Checksum is mandated on critical control messages and provisional on the remainder of the messages. Implementing this level of error detection ensures a higher degree of error free data integrity requirements than only odd parity provides.

The 1760 option implements:

Checksum generation and checksum error detection capabilities. Checksums are computed as each Data Word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last Data Word. On an incoming message, the computed checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

Checksum error injection in BC/Concurrent-RT mode. The user can set the checksum to intentionally send an error, giving the additional capability to test for checksum errors on the receiving RTs.

Header Words for message identification. The first Data Word of a message may be a Header Word. The Header Word is associated with a specific RT subaddress.

For more details see the sections on 1760 options in **Chapter 2: Remote Terminal Operation** and **Chapter 3: BC/Concurrent-RT Operation**.

To order the *M4K1553Px* with the 1760 option, see **Chapter 8: Ordering Information.**

1.1.4 Single Function Option (*PxS*)

The *PxS* is a single function version of the standard *Px* module. It operates as a single Remote Terminal (RT), a Bus Controller (BC) or Triggerable Bus Monitor, with an Internal Concurrent monitor for RT and BC operation.

The differences between the standard *Px* module and the single function module are as follows:

- The *PxS* simulates only one RT at a time.
- It does not support BC/Concurrent-RT mode.
- It has a fixed amplitude.
- It has no error injection capability.
- It has only one LED (see **7.2 LED Indicators** on page 7-2).
- The single RT address is provided via the RT Number register (see **2.11.1 RT Number Register (PxS Only)** on page 2-18) with an option to set the RT address via the module connector.
- In several of the RT mode tables, only the first word (or byte) is used; the rest is reserved (see **2.2 RT Memory Map** on page 2-4).
- Illegalization is done based on the SAid, not the RTid, using the Broadcast SAid Control Table (see **2.11.6 Broadcast SAid Control Table (PxS Only)** on page 2-20).

1.2 Installation

For hardware and software installation instructions, see the **`readme.pdf`** file on the root folder of the installation CD. When downloading new software from the Excalibur website, the **`readme.pdf`** file is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see the **`readme.pdf`** file. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.2.1 Module Installation

Warning Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur module.

1. If the module is supplied separately from the carrier board, *very carefully*, insert the module on the carrier *EXC-4000* board. The pin #1 marker (marked with a white rectangle) on the module must be aligned with the white rectangles on the carrier board.
2. 1553 devices may be connected via the I/O connector on the carrier board to the 1553 bus either directly (Direct Coupled) or via a bus-coupling stub (Transformer Coupled). Use DIP switches SW1 and SW2 to set the coupling mode to the 1553 bus(es). See **7.3 Module Coupling Mode Select DIP Switches** on page 7-2.

3. With the computer power source switched **off**, insert the *EXC-4000* carrier board with the *M4K1553Px* module into a slot in the computer.
4. Attach the 1553 adapter cable to the carrier board I/O connector and to the bus.

Important The cables may be connected to or disconnected from the board while power to the computer is turned on but *not* while the board is transmitting over the bus.

1.3 1553 Bus Connections

For short distances, the *M4K1553Px* may be coupled directly to another 1553 device. To ensure data integrity, make certain that the cable connecting the two devices is properly terminated with 78-Ohm resistors. See Figure 1-2 **Direct Coupled Connection (one bus shown)**.

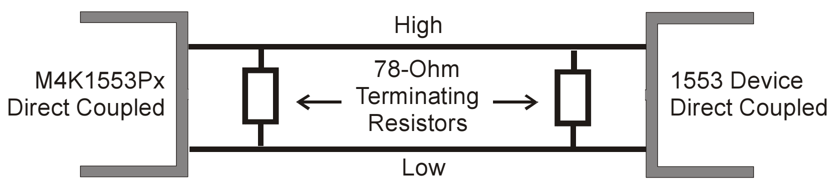


Figure 1-2 Direct Coupled Connection (one bus shown)

If operating in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems. Two terminators are required for each coupler, which services a single bus, i.e. BUS A. See Figure 1-3 **Transformer Coupled Connection (one bus shown)**.

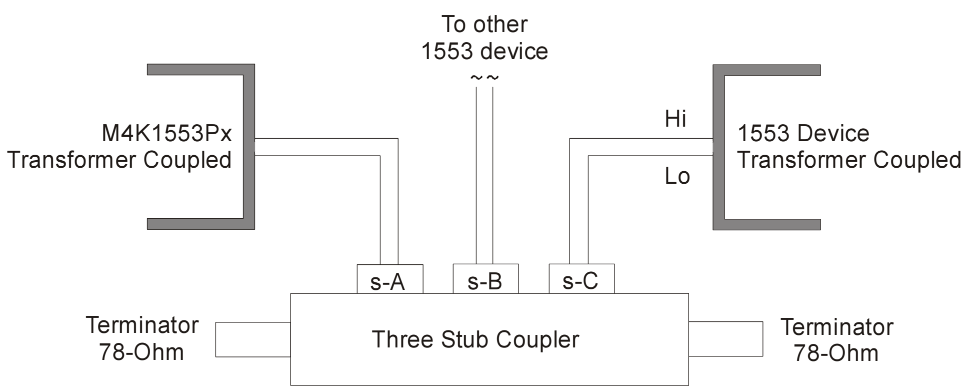


Figure 1-3 Transformer Coupled Connection (one bus shown)

For more information see our website: www.mil-1553.com.

Example of MIL-STD-1553 Bus Connection

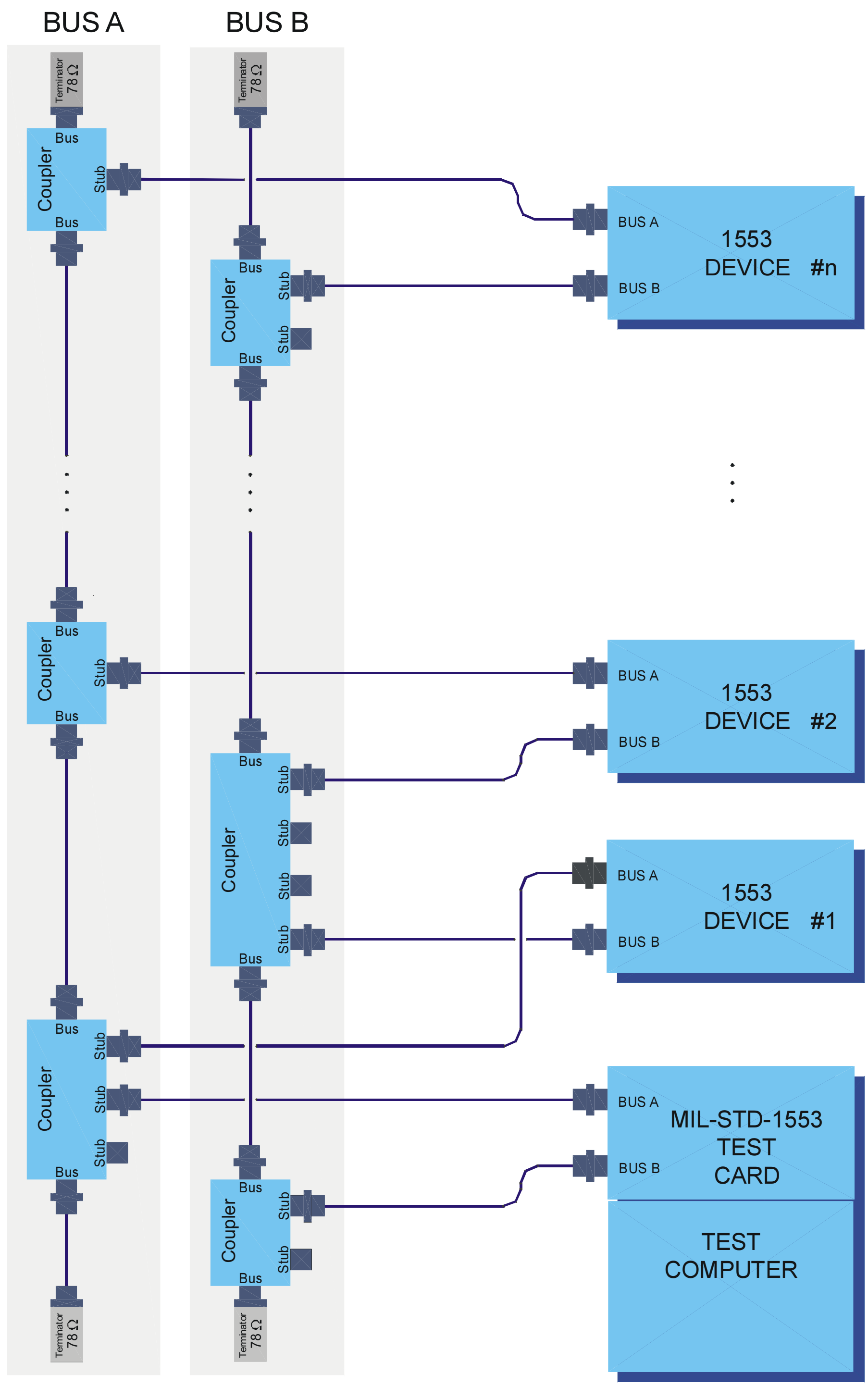


Figure 1-4 MIL-STD-1553 Bus Connection

1.4 *M4K1553Px* General Memory Map

The *M4K1553Px* occupies 64K bytes of the module's 128K-memory space. These 64K bytes are shared between the Control registers and the Data Block.

Mode Specific Registers	7010 – FFFF H
Hardware Revision Register	700E – 700F H
Mode Specific Registers	700C – 700D H
Time Tag (Hi)	700A – 700B H
Time Tag (Lo)	7008 – 7009 H
Time Tag Reset Register	7007 H
Mode Specific Registers	7001 – 7006 H
Module Reset Register	7000 H
Mode Specific Registers	4000 – 6FFF H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3 FFC H
Mode Specific Registers	3E86 – 3FFB H
Module Options Register	3E84 – 3E85 H
Reserved	3E81 – 3E83 H
Firmware Revision Register	3E80
Mode Specific Registers	0000 – 3E7F H

Figure 1-5 *M4K1553Px* General Memory Map for PCI[e] Carrier Boards

Chapters 2 to 4 of the *User's Manual* explain the operation of the *M4K1553Px* module in each of the three modes: Remote Terminal, BC/Concurrent RT and Bus Monitor. In each chapter the mode specific Memory Map and Control registers are described. Chapter 5 covers BC/Concurrent-RT operation.

1.5 VME/VXI Byte Swapping

When the module is installed on an Excalibur 4000 PCI family carrier board, all 8-bit registers and 8-bit memory locations can be found in the locations described in this manual.

When the module is installed on an *EXC-4000VME/VXI* carrier board, all 8-bit registers and 8-bit memory locations may be byte swapped. That is, during any individual 8-bit read or write operation to these registers, the even addresses may be swapped with the odd address (and vice versa) within a single 16-bit boundary (one word). This does not occur for 16-bit read/write operations.

For example:

PCI[e] Carrier Boards

BC Response Time Register	3FF3 H
Variable Amplitude Register	3FF2 H

VME/VXI Carrier Boards

Variable Amplitude Register	3FF3 H
BC Response Time Register	3FF2 H

1.6 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

2 Remote Terminal Operation

Chapter 2 describes module operation in Remote Terminal (RT) mode. The following topics are covered:

2.1 RT Mode Overview

Each multifunction module can be configured to simulate up to 32 remote terminals. The user selects which terminal or terminals are active and can inject errors into message responses. The single function module (*PxS*) simulates only one RT and does not support error injection. For more information on the single function module, see **1.1.4 Single Function Option (PxS)** on page 1-5.

After receiving the Start command, the module handles the transfer of all messages. See **2.11 Control Register Definitions** on page 2-18. Data associated with a particular RT subaddress combination is transferred via a 2K × 8 Look-up Table, which points to one of 256 Data Blocks (512 when using Expanded Block mode). The user loads Data Blocks associated with transmit commands with 1553 data to transmit, and reads received 1553 data from Data Blocks associated with receive commands.

The module will respond properly to messages received with an intermessage gap time of 4 µsec.

The user can choose whether the remote terminal should transmit its 1553 Status Word at the end of a message, even if the message contains *invalid* Data Words (invalid as specified by MIL-STD-1553). Use the RT Protocol Options register, to activate or disable this feature. See **2.11.19 RT Protocol Options Register** on page 2-28.

The remote terminal transmits its 1553 Status Word in approximately 4 µsec. Use the RT Response Time register to increase the time it takes the remote terminal to transmit the 1553 Status Word.

Since most 1553 parameters, such as response time, Status Word content, etc. are user programmable, the module can operate in various 1553 environments. The module also allows you to enable or disable the 1553 Broadcast function. If broadcasting is enabled, RT address 31 (11111) is reserved; if broadcasting is disabled, all 32 RT addresses are available. See **2.11.21 Broadcast Control Register** on page 2-29.

The 1553 Mode Code subaddress identifier can be programmed (see **2.11.42 Mode Code Control Register** on page 2-37) so that either 31, 0, or both are used to indicate that the 1553 Command Word is a Mode Code.

To determine whether the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID register (test for value = 45 H)
2. Check the Module Status register (test for Module Ready bit = 1)

The module is installed and ready when both registers contain the correct values, as written above. For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a ‘1’ to the Start register is referred to as “issuing a Start command”.

2.2 RT Memory Map

The following memory maps show addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

When Using the Expanded Data Block Option (512 Blocks Total)

Expanded Data Block Area (256 Additional Blocks)	C000 – FFFF H
Internal Concurrent Monitor Message Block Area[1]	8000 – BFFF H

When Using the Default Data Block Option

Internal Concurrent Monitor Message Block Area[1]	8000 – FFFF H
1553 Data Blocks (56 Additional Blocks)	7200 – 7FFF H
Reserved	7022 – 71FF H
RT Number Register[3]	7020 – 7021 H
Reserved	700C – 7019 H
Time Tag (Hi)	700A – 700B H
Time Tag (Lo)	7008 – 7009 H
Time Tag Reset Register	7007 H
Reserved	7004 – 7006 H
Options Select Register	7003 H
Reserved	7001 – 7002 H
Module Reset Register	7000 H
RT Message Stack (512 blocks)	6000 – 6FFF H
Broadcast SAid Control Table[3]	5800 – 5FFF H
RTid Control Table	4800 – 57FF H
Data Block Look-up Table	4000 – 47FF H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3FFC H
Message Received Status Register	3FFB H
Reserved	3FF8 – 3FFA H
Time Tag Resolution Register	3FF7 H
Bit Count Register	3FF6 H
Reserved	3FF5 H
RT Response Time Register	3FF4 H
Error Injection Register	3FF3 H
Variable Amplitude Register[5]	3FF2 H
Old RT Message Stack Pointer	3FF0 – 3FF1 H
RT Protocol Options Register	3FEF H
Reserved	3FEC – 3FEE H
Module Function Register	3FEA – 3FEB H
Broadcast Control Register	3FE8 – 3FE9 H
Reserved	3F80 – 3FE7 H
1760 Header Value Transmit Table[2]	3F40 – 3F7F H
1760 Header Value Receive Table[2]	3F00 – 3F3F H

1760 Header Exist Table[2]	3EC0 – 3EFF H
RT Message Stack Pointer	3EBE – 3EBF H
Reserved	3EA6 – 3EBD H
Module Time Register (Lo)	3EA4 – 3EA5 H
Module Time Register (Hi)	3EA2 – 3EA3 H
Serial Number Register	3EA0 – 3EA1 H
Error Counter (Lo)	3E9E – 3E9F H
Error Counter (Hi)	3E9C – 3E9D H
Message Counter (Lo)	3E9A – 3E9B H
Message Counter (Hi)	3E98 – 3E99 H
Reserved	3E96 – 3E97 H
RTid with Bad Block Number Register	3E94 – 3E95 H
Bad Block Number Register	3E92 – 3E93 H
Internal Concurrent Monitor Next Message Pointer[1]	3E90 – 3E91 H
Reserved	3E8A – 3E8F H
Clear Time Tag on Sync Register	3E88 – 3E89 H
More Module Options Register	3E86 – 3E87 H
Module Options Register	3E84 – 3E85 H
Reserved	3E81 – 3E83 H
Firmware Revision Register	3E80 H
Reserved	34C0 – 3E7F H
1553 RT Vector Word Table[4]	3480 – 34BF H
1553 RT BIT Word Table[4]	3440 – 347F H
RT Last Command Word Table[4]	3400 – 343F H
Reserved	33FD – 33FF H
Interrupt Condition Register	33FC H
Old RT Message Stack (42 blocks)	3300 – 33FB H
Word Count Error Table[5]	32E0 – 32FF H
Reserved	3267 – 32DF H
Mode Code Control Register	3266 H
1760 Checksum Limits Register[2]	3264 – 3265 H
Reserved	3260 – 3263 H
1553 RT Status Word Table[4]	3220 – 325F H
RT Settings Table[4]	3200 – 321F H
1553 Data Blocks (200 Blocks)	0000 – 31FF H

Figure 2-1RT Memory Map for PCI[e] Carrier Boards

1. See **Chapter 5: Internal Concurrent Monitor**
2. Only for 1760 option
3. Only for single function module (*PxS*); in a multifunction module this register is reserved
4. On a single function module (*PxS*) only the first location is used; the rest are reserved
5. On a single function module (*PxS*) this register is reserved

When Using the Expanded Data Block Option (512 Blocks Total)

Expanded Data Block Area (256 Additional Blocks)	C000 – FFFF H
Internal Concurrent Monitor Message Block Area[1]	8000 – BFFF H

When Using the Default Data Block Option

Internal Concurrent Monitor Message Block Area[1]	8000 – FFFF H
1553 Data Blocks (56 Additional Blocks)	7200 – 7FFF H
Reserved	7022 – 71FF H
RT Number Register[3]	7020 – 7021 H
Reserved	700C – 7019 H
Time Tag (Hi)	700A – 700B H
Time Tag (Lo)	7008 – 7009 H
Reserved	7007 H
Time Tag Reset Register	7006 H
Reserved	7003 – 7005 H
Options Select Register	7002 H
Module Reset Register	7001 H
Reserved	7000 H
RT Message Stack (512 blocks)	6000 – 6FFF H
Broadcast SAid Control Table[3]	5800 – 5FFF H
RTid Control Table	4800 – 57FF H
Data Block Look-up Table	4000 – 47FF H
Module ID Register	3FFF H
Module Configuration Register	3FFE H
Start Register	3FFD H
Module Status Register	3FFC H
Reserved	3FFB H
Message Received Status Register	3FFA H
Reserved	3FF8 – 3FF9 H
Bit Count Register	3FF7 H
Time Tag Resolution Register	3FF6 H
RT Response Time Register	3FF5 H
Reserved	3FF4 H
Variable Amplitude Register[5]	3FF3
Error Injection Register	3FF2 H
Old RT Message Stack Pointer	3FF0 – 3FF1 H
Reserved	3FEF H
RT Protocol Options Register	3FEE H
Reserved	3FEC – 3FED H
Module Function Register	3FEA – 3FEB H
Broadcast Control Register	3FE8 – 3FE9 H
Reserved	3F80 – 3FE7 H
1760 Header Value Transmit Table[2]	3F40 – 3F7F H
1760 Header Value Receive Table[2]	3F00 – 3F3F H

1760 Header Exist Table[2]	3EC0 – 3EFF H
RT Message Stack Pointer	3EBE – 3EBF H
Reserved	3EA6 – 3EBD
Module Time Register (Lo)	3EA4 – 3EA5 H
Module Time Register (Hi)	3EA2 – 3EA3 H
Serial Number Register	3EA0 – 3EA1 H
Error Counter (Lo)	3E9E – 3E9F H
Error Counter (Hi)	3E9C – 3E9D H
Message Counter (Lo)	3E9A – 3E9B H
Message Counter (Hi)	3E98 – 3E99 H
Reserved	3E96 – 3E97 H
RTid with Bad Block Number Register	3E94 – 3E95 H
Bad Block Number Register	3E92 – 3E93 H
Internal Concurrent Monitor Next Message Pointer[1]	3E90 – 3E91 H
Reserved	3E8A – 3E8F H
Clear Time Tag on Sync Register	3E88 – 3E89 H
More Module Options Register	3E86 – 3E87 H
Module Options Register	3E84 – 3E85 H
Reserved	3E82 – 3E83 H
Firmware Revision Register	3E81 H
Reserved	34C0 – 3E80 H
1553 RT Vector Word Table[4]	3480 – 34BF H
1553 RT BIT Word Table[4]	3440 – 347F H
RT Last Command Word Table[4]	3400 – 343F H
Reserved	33FE – 33FF H
Interrupt Condition Register	33FD H
Reserved	33FC H
Old RT Message Stack (42 blocks)	3300 – 33FB H
Word Count Error Table[5]	32E0 – 32FF H
Reserved	3268 – 32DF H
Mode Code Control Register	3267 H
Reserved	3266 H
1760 Checksum Limits Register[2]	3264 – 3265 H
Reserved	3260 – 3263 H
1553 RT Status Word Table[4]	3220 – 325F H
RT Settings Table[4]	3200 – 321F H
1553 Data Blocks (200 Blocks)	0000 – 31FF H

Figure 2-2RT Memory Map for VME/VXI Carrier Boards

1. See **Chapter 5: Internal Concurrent Monitor**
2. Only for 1760 option
3. Only for single function module (*PxS*); in a multifunction module this register is reserved
4. On a single function module (*PxS*) only the first location is used; the rest is reserved
5. On a single function module (*PxS*) this register is reserved

2.3 Data Block Look-up Table

2.3.1 Data Block Look-up Table for Multifunction Modules

When a command is received by the module, the RTid, which consists of the RT Address, T/R Bit and the Subaddress of the Command Word, is used to index the datablock Look-up Table and get the datablock number that the user assigned to the RTid. (For more details on RTid, see **2.3.1.3 RT Identifier (RTid)** on page 2-8.) The Data Block Look-up Table is located at 4000 – 47FF (H).

The user assigns datablocks to transmit RTids (and uses the datablock to set data to be sent out by this RTid) and receive RTids (the module will store data received by the RTid in this datablock) by filling in the corresponding entry in the datablock Look-up Table as shown in the table below.

Note: Data Block 0 represents a default for all unassigned RTids and is not recommended for use by anyone interested in using the data. If an RTid does not have a Data Block assigned to it, the default Data Block (0) is used for both receive and transmit messages.

	RTid (11 most significant bits of the 1553 Command Word)					
Base Address	**RT address (5 bits)**	**T/R (1 bit)**	**Sub-address (5 bits)**	**Look-up table (2K x 8)**	**Data Block Storage Area**	**Address of Data Block**
4000+	11111	1	11111	Block #	Data Block 511	FFFF H
	•	•	•	•	•	•
					256	C000 H
					255	7FFF H
	•	•	•	•	•	•
					200	7200 H
					199	31C0 H
	•	•	•	•	•	•
4000+	00000	0	00001	Block #	Data Block 1	0040 H
4000+	00000	0	00000	Block #	Data Block 0	0000 H

Figure 2-3 Data Block Look-up Table for Multifunction Modules

2.3.1.1 Data Block Storage Areas

There are 512 datablocks available. Each block contains 32 1553 Data Words (64 bytes). Data Block 0 begins at address 0000. Data Block 1 begins at address 0040 (H), etc.

- 0 – 199 are stored in consecutive addresses, starting at address 0000 H.
- 200 – 255 are stored in consecutive addresses, starting at address 7200 H.
- 256 – 511 are stored in consecutive addresses, starting at address C000 H (available only in Expanded Block mode).

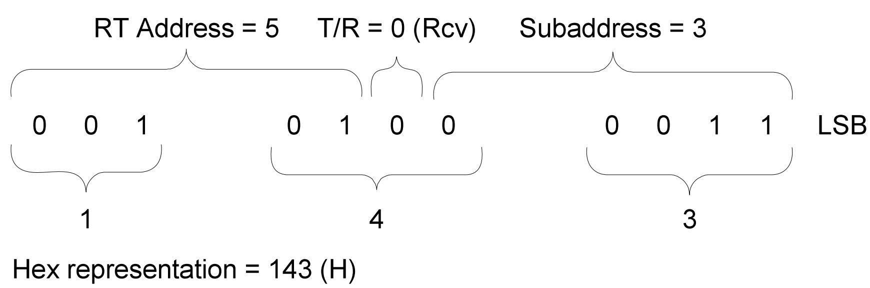
When Expanded Block mode is disabled, there are 256 available datablocks. When Expanded Block mode is enabled, 512 datablocks are available, but the Internal Concurrent Monitor message area is reduced from 409 to 204 messages.

In order to use Expanded Block mode, it must be enabled via the Module Function register. See **2.11.20 Module Function Register** on page 2-29. In addition, set Bit 06 of the corresponding RTid entry in the RTid Control Table (0040 H) to 1. This adds an additional high bit (a value of 256) to the number found in the corresponding RTid entry in the Look-up table. For example, if an RTid is assigned to block number 100, the RTid is now assigned to block number 356. See **2.11.7 RTid Control Table** on page 2-21.

To create an address to a Look-up table:

1. Isolate the eleven most significant bits of the 1553 Command Word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a Data Block for a 1553 receive message to RT#5, Subaddress 3.



2. Add the Hex value of this part of the Command Word to the base address of the Look-up table (4000 H).

4000	(H)
+143	(H)
4143	(H)

3. Write the Data Block number to address 4143 H.

Example: `POKE &H4143,01` allocates block #1 for the data of this message. Read the 1553 data out by reading block #1, which starts at address 0040 (H). Each Data Block, beginning at address 0000 is 64 bytes long (for up to 32 1553 Data Words). The address of a block is obtained by multiplying its block number by 64 (40 H).

2.3.1.2 Data Storage

Within a specific Data Block, the 1553 Data Words must be stored and/or read in the following format:

1553 Word #N	Last Location in Data Block
• • •	
1553 Word #2	
1553 Word #1	First Location in Data Block

Figure 2-4 Data Storage Sequence

2.3.1.3 RT Identifier (RTid)

The RTid is referred to frequently in the RT Control registers. The RTid is defined as an RT address, T/R bit value and RT subaddress combination. The structure of the RTid is illustrated below:

5 bits	1 bit	5 bits
RT ADDRESS	T/R[1]	SUBADDRESS

RT Identifier

1. Transmit = 1 / Receive = 0

Example: RT#5, Transmit, Subaddress 6 would be represented as 00101 1 00110 (0166 H). This value can be isolated from a Command Word by shifting the Command Word 5 bits to the right.

Mode Codes: In the case of Mode Code the last 5 bits signify the Mode Code instead of the Subaddress.

See **To create an address to a Look-up table:** on page 2-7.

2.3.2 Data Block Look-up Table for Single Function (*PxS*) Modules

When a command is received by the module, the SAid, which consists of the T/R Bit, Subaddress and Word Count, is used to index the datablock Look-up Table and get the datablock number that the user assigned to the SAid. (For more details on SAid, see **2.3.2.3 Subaddress Identifier (SAid)** on page 2-10.) The Data Block Look-up Table is located at 4000 – 47FF (H).

The user assigns datablocks to transmit SAids (and uses the datablock to set data to be sent out by this SAid) and receive SAids (the module will store data received by the SAid in this datablock) by filling in the corresponding entry in the datablock Look-up Table as shown in the tables below.

Note: Data Block 0 represents a default for all unassigned SAids and is not recommended for use by anyone interested in using the data. If an SAid does not have a Data Block assigned to it, the default Data Block (0) is used for both receive and transmit messages.

	SAid (11 least significant bits of the 1553 Command Word)					
Base Address	T/R (1 bit)	Sub-address (5 bits)	Word Count (5 bits)	Look-up table (2K x 8)	Data Block Storage Area	Address of Data Block
4000+	1	11111	11111	Block #	Data Block 511	FFFF H
	•	•	•	•	•	•
					256	C000 H
					255	7FFF H
	•	•	•	•	•	•
					200	7200 H
					199	31C0 H
	•	•	•	•	•	•
4000+	0	00001	00000	Block #	Data Block 1	0040 H
4000+	0	00000	00000	Block #	Data Block 0	0000 H

Figure 2-5 Data Block Look-up Table for Single Function (*PxS*) Modules

2.3.2.1 Data Block Storage Areas

The Data Block Storage Areas for the single function (*PxS*) module are the same as the multifuction module, except that they use the SAid pointer instead of the RTid. See **2.3.1.1 Data Block Storage Areas** on page 2-7.

2.3.2.2 Data Storage

Data storage for the single function (*PXS*) module is the same as the multifuction module. See **2.3.1.2 Data Storage** on page 2-8.

2.3.2.3 Subaddress Identifier (SAid)

The SAid is defined as a T/R bit, subaddress and word count combination. The structure of the SAid is illustrated below:

1 bit	5 bits	5 bits
T/R[1]	SUBADDRESS	WORD COUNT

Subaddress Identifier

1. Transmit = 1 / Receive = 0

Example: Transmit, Subaddress 6, Word Count 5 would be represented as 1 00110 00101 (04C5 H). This value can be isolated from a Command word by masking out the upper 5 bits (for example, Command word & 07FF H).

2.4 RT Settings Table

2.4.1 RT Settings Table for Multifunction Modules

The 32 locations (bytes) of the RT Settings table (3200 – 321F H) contains settings for each remote terminal, including which RTs are active. The first byte in the RT Settings table relates to RT #0, the next to RT #1, and the last location relates to RT #31.

To set RT as active, set Bit 00 of the corresponding RT Settings byte to logic 1.

RT#31 Settings Byte	32nd byte	321F H
• • •	• • •	• • •
RT#0 Settings Byte	1st byte	3200 H

Figure 2-6 RT Settings Table for Multifunction Modules – RT Mode

Note: When operating in Broadcast mode, the active RT Look-up Table entry must be set for RT#31 as Not Active.

The following table describes the bits in each byte in the RT Settings table.

Bit	Bit Name	Description
05-07	**0**	Reserved
04	**Status Word Duration**	1 = One time 0 = Always This bit determines the duration of user-defined 1553 RT Status Word. If this bit is set to 1, the user-defined Status Word for this RT is used only one time. Then all user-defined bits are cleared (only the RT address field remains as set). See **2.11.44 1553 RT Status Word Table** on page 2-38.
03	**Inactive Bus B**	1 = Bus B Inactive 0 = Bus B Active If Bit 00 is set to 1 and Bit 03 is set to 0, the module will respond to all messages received over bus B for this RT. If Bit 03 is set to 1, all messages over bus B for this RT will be ignored.
02	**Inactive Bus A**	1 = Bus A Inactive 0 = Bus A Active If Bit 00 is set to 1 and Bit 02 is set to 0, the module will respond to all messages received over bus A for this RT. If Bit 02 is set to 1, all messages over bus A for this RT will be ignored.
01	**Interrupt**	1 = Interrupt 0 = No Interrupt If Bit 01 is set to 1, if the RT is active and the Interrupt Condition register is enabled, then this module will generate an interrupt as per the Interrupt Condition register. See **2.11.39 Interrupt Condition Register** on page 2-35. **Note:** If the interrupt bit is set in the RT Settings Table, the interrupt setting in the RTid Control Table is ignored. To set an interrupt at the RTid level, make sure the interrupt bit in the RT Settings Table is disabled.
00	**Active**	1 = RT Active 0 = RT Not Active If Bit 00 is set to 0, the RT is not active, and none of the other bit settings are relevant. If it is set to 1, the other bits are checked. **Note:** On a single function module (*PxS*), this bit is reserved.

RT Settings Byte

2.4.2 RT Settings Table for Single Function (*PxS*) Modules

On a single function module (*PxS*), the first byte (3200 H) is for the RT settings of the active RT and the fifth byte (3204 H) shows the RT number of the active RT. The rest of the bytes are reserved. (The active RT is selected via the RT Number register. See **2.11.1 RT Number Register (PxS Only)** on page 2-18.).

Reserved	3205 – 321F H
Active RT Number Byte (read only)	3204 H
Reserved	3201 – 3203 H
RT Settings Byte	3200 H

Figure 2-7 RT Settings Table for Single Function (*PxS*) Modules – RT Mode

The bits of the RT Settings byte are the same as for multifunction modules. See page 2-11.

2.4.2.1 Active RT Number

The following table describes the bits of the Active RT Number Byte.

Bit	Description
05-07	Reserved
00-04	The number of the active RT

Active RT Number

2.5 RT Message Stack

The RT Message Stack is located at 6000 – 6FFF H.

In RT mode, the module generates a message stack in the dual-port RAM. This stack contains information used for post-processing of RT messages. The stack is divided into 512 blocks, each containing four words, including a 32-bit Time Tag value. The stack operates as a circular buffer. Only messages relating to active RTs are stored, **Figure 2-8** illustrates one block. The RT Message Stack pointer points to the beginning of the next unused block. See **2.11.25 RT Message Stack Pointer** on page 2-31.

	Byte Offset
Message Status Word	+6
Time Tag Word Lo	+4
Time Tag Word Hi	+2
1553 Command Word	0

Figure 2-8 RT Message Stack Block Structure

How the Module Updates an RT-to-RT Message

When an RT-to-RT message is received, where the module is functioning as both RTs, the message stack is updated as follows:

Two message stack blocks are utilized.

1. The 1553 Receive Command Word is written into the *first* message stack block.
2. The 1553 Transmit Command Word and Message Status Word are written into the second stack block.
3. The Message Status Word is written into the first (Receive) message stack block.

Both the Receive side and Transmit side message stack blocks contain the identical Message Status Word, with the RT-to-RT bit set to 1, and the same Time Tag Word.

2.5.1 Old RT Message Stack

The original *Px* module had a single message stack with 42 message entries and a 16-bit Time Tag. In later versions of the *Px* module, a new message stack was added with 512 message entries and a 32-bit Time Tag.

For new applications it is recommended only to use the new message stack. However, for backward compatibility the old message stack is available. It is located in the dual-port RAM at 3300 – 33FB (H) and is divided into 42 blocks each containing 3 words, including a 16-bit Time Tag value which is the lower 16-bits of the 32-bit Time Tag Counter. The pointer to this stack is at 3FF0 (H).

Currently only the new message stack is enabled by default. To enable the old message stack, set Bit 02 of the RT Protocol Options register. See **2.11.19 RT Protocol Options Register** on page 2-28.

2.5.1.1 Determining Your Module's RT Message Stack Configuration

You can determine your module's message stack behavior by checking the module revision number printed on the module itself or by checking the firmware revision. See **2.11.35 Firmware Revision Register** on page 2-34. For module revision C, check the firmware revision and refer to the table below to determine whether the new message stack exists.

Module Revision	Firmware Revision	Message Stack Details
A, A1	4.x – 6.9	Only one stack exists with 42 message entries
C	From 1.0 – 1.6	Only one stack exists with 42 message entries
	From 1.7 – 3.3	Both new and old message stacks are enabled
D or later	8.0 or later	By default only the new stack is enabled (512 message entries).

2.5.2 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the 1553 Status Word (see **2.11.44 1553 RT Status Word Table** on page 2-38). The contents of the Message Status Word are:

Bit	Bit Name	Description
15	End of Message	Message transfer completed
14	Bus A / B	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
13	1760 Checksum Error	The calculated checksum (on an incoming message) does not match the last Data Word received
11 – 12	Reserved	Set to 0
10	Tx Time Out	Module, acting as receiver in RT-to-RT message, did not sense a transmitter Status Word (in 14 μsec.)
09	Superseding	A new command word to the same RT was detected in middle of receiving this message. The new command will be placed in the following message stack entry.
08	1760 Header Error	Header Word received does not match the value set in the Header Value table. See **2.9.1 Header Word** on page 2-16.
07	Invalid Word Received	At least one invalid 1553 Word received (i.e. bit count, Manchester code, parity)
06	Reserved	Set to 0
05	Word Count Error (Receive Message)	Incorrect number of words received in the message
04	Broadcast Message	Broadcast Command Word received
03	Incorrect Sync Received	Sync of either the Status or the Data Word(s) is incorrect
02	Non- Contiguous Data (Receive Message)	Invalid gap between received 1553 Words
01	RT-RT Message	RT-to-RT message received
00	Error	Error occurred (The error type is defined in one of the other message status bit locations)

Remote Terminal Message Status Word

Note: A logic 1 indicates the occurrence of a status flag

The Message Status Word is valid only when Bit 15, End of Message, is turned on.

2.5.3 Time Tag

Read only The Time Tag value is a 32-bit word that can be used to determine the time elapsed since reset. The Time Tag uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution register. The equation to determine the Time Tag resolution = (Time Tag Resolution register value + 1) × 4 µsec.

Example:

Time Tag Resolution register value = 0 → Counter's resolution = 4 µsec
Time Tag Resolution register value = 4 → Counter's resolution = 20 µsec

To reset the Time Tag counter (to 0) any time, write to the Time Tag Reset register. See **2.11.3 Time Tag Reset Register** on page 2-19.

When the first command of each message is received, the value of the 32-bit Time Tag Counter register is written to dual-port RAM.

Note: The counter's value can be read at any time by reading the Time Tag counter addresses. (See **2.11.2 Time Tag Counter** on page 2-19.)

Example: How To Calculate Elapsed Time

Time Tag Resolution register = 03 (initialized before Start command)

Time Tag values (read during or after message transfers):

Low = 0040 (H)
High = 0010 (H)

Time elapsed since Start command
= (Time Tag register value) × (Time Tag Resolution value + 1) × (4 µsec)
= 100040 (H) × (03 + 1) × 4 µsec
= 1048640(Dec) × (4 × 4 µsec) = 16778240 µsec (16778.24 msec. = 16.778 sec.)

2.5.4 1553 Command Word

The Command Word location contains the 1553 Command Word associated with the message.

Only active RT Command Words are stored.

2.6 Mode Codes

The user can program the Subaddress code that will indicate that a Mode command has been received. Either or both of the following codes can be used: 11111 and 00000. The Mode Code Control register must be programmed as described in section **2.11.42 Mode Code Control Register** on page 2-37.

The module handles all dual-redundant 1553B Mode Codes. The Word Count field is decoded according to MIL-STD-1553B. One of the Mode Codes (Synchronize with Data Word) is operated upon as a standard message transfer, using the Data Block Look-up Table. When the module encounters the Synchronize with Data Word Mode Code, the Command Word's RT Address, T/R bit, and Subaddress fields are used as a pointer to the Look-up Table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0 – 255) indicating where the Synchronize with Data Word's data word should be stored.

The data associated with Mode Codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the dual-port RAM (described in **2.11.38 RT Last Command Word Table**, **2.11.37 1553 RT BIT Word Table**, and **2.11.36 1553 RT Vector Word Table** on page 2-34).

2.7 Broadcast Mode

To operate the module in Broadcast mode, select the appropriate bit settings as defined in **2.11.21 Broadcast Control Register** on page 2-29.

When operating in Broadcast mode, the active RT Look-up Table entry must be set for RT#31 as Not Active. The module reads the Broadcast Control register to determine whether the module is operating in Broadcast mode.

In Broadcast mode, the module stores the received message in a 1553 Data Block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block Look-up Table memory.

2.8 Error Injection Feature

The module allows two types of error injection:

- **Global (for all RTs)** – The global errors such as Sync and Non-Contiguous data are described in **2.11.16 Error Injection Register** on page 2-27. These errors are either ON or OFF for all RTs.
- **Per RT** – The ability to inject a 1553 Word Count error can be set per RT using the Word Count Error table. See **2.11.41 Word Count Error Table** on page 2-36.

Note: Error injection is not available on a single function module (*PxS*).

2.9 1760 Options

2.9.1 Header Word

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific Subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the Header Exist table to 1. Then set the corresponding entry in the Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default module setting, or another value the user enters in the Header Value Transmit/Receive Table. The module checks that the specified Header receive value was received. In addition, the Internal Concurrent Monitor checks that the specified Header transmit/receive value was received. If the wrong data was received, the **1760 Header error** bit is set in the Message Status Word. See **2.5.2 Message Status Word** on page 2-14.

See **2.11.22 1760 Header Value Transmit Table**, **2.11.23 1760 Header Value Receive Table** and **2.11.24 1760 Header Exist Table** on page 2-31.

2.9.2 1760 Checksum Error

MIL-STD-1760 implements checksum error detection capabilities. Checksums are calculated as each Data Word is received. Upon an incoming message, the calculated checksum is compared to the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

Note: Error injection is not available on a single function module (*PxS*).

2.10 Program Example: RT Mode

The following two programming examples use the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

All values are in Hex unless otherwise states.

BASIC Instruction	Remarks
`10 POKE &H3FFF,02`	Set the Configuration register to RT mode
`20 POKE &H3FF2,xx`	Set the Variable Amplitude register
`30 POKE &H3201,1`	Enable RT #1
`40 POKE &H3204,1`	Enable RT #4
`50 POKE &H3222,00`	Set the Status Word of RT #1 to 0800
`60 POKE &H3223,08`	
`70 POKE &H3228,00`	Set the Status Word of RT #4 to 2000
`80 POKE &H3229,&H20`	
`90 POKE &H3FF7,xx`	Set the Time Tag Resolution register
`100 POKE &H3266,00`	Set the Mode Code Control register to Subaddress 0 & 31
`110 POKE &H3FF3,00`	Set No global error injection
`120 POKE &H4xxx,1`	Load block number 1 for data storage into Look-up table xxx
`130 POKE &H4yyy,2`	Load block number 2 for data storage into Look-up table yyy
`140 POKE &H3FFC,1`	Set the Start register to 1 to start RT mode
`150 STOP`	

Program Example for PCI[e] Carrier Boards – RT Mode

BASIC Instruction	Remarks
`10 POKE &H3FFE,02`	Set the Configuration register to RT mode
`30 POKE &H3200,1`	Enable RT #1
`40 POKE &H3205,1`	Enable RT #4
`50 POKE &H3223,00`	Set the Status Word of RT #1 to 0800
`60 POKE &H3222,08`	
`70 POKE &H3229,00`	Set the Status Word of RT #4 to 2000
`80 POKE &H3228,&H20`	
`90 POKE &H3FF6,xx`	Set the Time Tag Resolution register
`100 POKE &H3267,00`	Set the Mode Code Control register to Subaddress 0 & 31
`110 POKE &H3FF2,00`	Set No global error injection
`120 POKE &H4xxx,1`	Load block number 1 for data storage into Look-up table xxx
`130 POKE &H4yyy,2`	Load block number 2 for data storage into Look-up table yyy
`140 POKE &H3FFD,1`	Set the Start register to 1 to start RT mode
`150 STOP`	

Program Example for VME/VXI Carrier Boards – RT mode

2.11 Control Register Definitions

2.11.1 RT Number Register (*PxS* Only) — Address: 7020 – 7021 (H)

The RT Number register contains the module's RT address and related information for a single function module (*PxS*).

Upon reset, bits 00 – 06 default to the values set by the module connector pins. (See **7.4.2 Module Terminal Stick Pin Assignments** on page 7-4.) To modify their values, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24). Bit 06 is a read only bit indicating whether the RT number is locked via a module connector pin, in which case the RT number cannot be modified.

Bit	Bit Name	Description
08 – 15	Reserved	
07	RTERR	0 = RT address parity OK 1 = RT address parity error **(Read only)**
06	RTLOCK	0 = RT number is unlocked and can be changed at any time 1 = RT number is locked and cannot be changed **(Read only)**
05	RTPTY	RT Address Parity Bit. This bit is appended to the remote terminal address bus to supply parity. Odd parity is required for proper operation.
00 – 04	RTNUM	RT Address Bits. These five bits contain the remote terminal address. 00 is the Least Significant Bit (LSB).

RT Number Register

2.11.2 Time Tag Counter

Address: 7008 – 700B (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset upon a power up or a software reset and starts counting. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

The counter must be read in the following sequence:

1. Read 7008 H – Lo word (16 bit, read only)
2. Read 700A H – Hi word (16 bit, read only)

The Time Tag resolution register sets the resolution of the counter. See **2.11.13 Time Tag Resolution Register** on page 2-25.

To calculate elapsed time between Time Tags:

Example:

1. The Time Tag Resolution register is set to 0. (See **2.11.13 Time Tag Resolution Register** on page 2-25.)
2. Calculate the Time Tag Resolution:
   (Time Tag Resolution register value + 1) × 4 = (0 + 1) × 4 = 4 µsec
3. Calculate difference between Time Tags:
   150 (Time Tag 2) – 50 (Time Tag 1) = 100
4. Elapsed time
   100 × 4 = 400 µsec

2.11.3 Time Tag Reset Register

Address: 7007 (H)

Write only

Write any value to the Time Tag Reset register to reset the module's Time Tag Counter. Immediately after the reset, the counter will start to count from 0.

2.11.4 Options Select Register

Address: 7003 (H)

Write only

Write to the Options Select register to select whether RT address 11111 (RT #31) is interpreted as a valid RT address or as a Broadcast address.

Bit	Description	
01 – 07	Reserved	
00	1	Broadcast option is active. RT#31 is Broadcast Address. No RT Status Word will be transmitted.
	0	Broadcast option is inactive, RT#31 is a regular RT. **Note:** Bit 00 has been retained for backward compatibility. For new application, use the Broadcast Control register instead. See **2.11.21 Broadcast Control Register** on page 2-29.

Options Select Register

Note: The Options Select register is reset at power-up (all bits set to 0) or by a module reset.

2.11.5 Module Reset Register **Address: 7000 (H)**

Write any value to the Module Reset register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, module ID and Firmware Revision registers are written by the module after the reset operation is completed.

2.11.6 Broadcast SAid Control Table (*PxS* Only) **Address: 5800 – 5FFF (H)**

The Broadcast SAid Control Table is a block of memory, one byte per SAid, to store SAid-specific settings, and to implement SAid-specific features.

	SAid (11 least significant bits of the 1553 Command Word)				
Base Address	**T/R (1 bit)**	**Subaddress (5 bits)**	**Word Count (5 bits)**	**Broadcast SAid Control table (2K x 8)**	
5800+	1	11111	11111	SAid Illegalization byte	5FFF H
	•	•	•	•	•
	•	•	•	•	•
	•	•	•	•	•
5800+	0	00000	00001	SAid Illegalization byte	5801 H
5800+	0	00000	00000	SAid Illegalization byte	5800 H

Figure 2-9 Broadcast SAid Control Table

Bit	Bit Name	Description
03 – 07	Reserved	
02	Illegalization	1 = The Message Error bit (Bit 10) is set in the 1553 RT Status Word of the next Mode Code 2 or Mode Code 18 message after the current BC-to-RT or Mode Code Message (see **2.11.44 1553 RT Status Word Table** on page 2-38).
00 – 01	Reserved	

Broadcast SAid Control Table Byte

Note: The Broadcast SAid Control Table is only for the single function module (*PxS*). On a multifunction module, this register is reserved.

2.11.7 RTid Control Table **Address: 4800 – 57FF (H)**

The RTid Control Table is a block of memory, one word per RTid, to store RTid-specific settings, and to implement RTid-specific features.

	RTid (11 most significant bits of the 1553 Command Word)					
Base Address	**RT address (5 bits)**	**T/R (1 bit)**	**Sub-address (5 bits)**	**Word Alignment[1]**	**RTid Control table (2K x 16)**	
4800+	11111	1	11111	0	RTid Information word	57FE H
	•	•	•	0	•	•
	•	•	•	0	•	•
	•	•	•	0	•	•
4800+	00000	0	00001	0	RTid Information word	4802 H
4800+	00000	0	00000	0	RTid Information word	4800 H

Figure 2-10 RTid Control Table

1. Additional bit for “even” addressing.

Bit	Bit Name	Description
12 – 15	Next Buffer	These bits are used for multibuffering. They contain the number of the next buffer to be used by the firmware, when either receiving or transmitting data. This field is updated by the module as soon as the processing of a command begins. For example, when the module begins processing a command using buffer 2, it updates the NextBuffer field to “3.” This field can be updated by the user, though care should be taken not to update it at the same time as the firmware, or the update could be lost. Initially, this field is set to “0” and is incremented by 1 for each successive use of the next buffer.
08 – 11	Multibuffers	These bits are written by the user to direct the firmware to use multibuffering. 0 = (**Default**) Multibuffering is turned off 1 = Two buffers are used 2 = Three buffers are used ... 15 = 16 buffers are used **Note:** Multibuffering can not be used together with double buffering (Bit 04); the user must select one mechanism or the other.
07	Reserved	
06	Expanded Data Block Bit	High order bit for block numbers above 255 (Expanded Block mode only)
05	Double buffer[1] datablock usage flag	The bit indicates which block of the double buffering pair to use for storing the data for this RTid. 0 = (**Default**) The module detects a receive message. The module stores the data at the even-numbered block number indicated in the Look-up Table. When the module completes writing all the Data Words to the block, the module sets this bit to 1. This indicates to write to the odd-numbered block the next time receive data comes in for this RTid. 1 = The module detects a receive message. The module stores the data at the odd-numbered block, whose number is one more than the even-number indicated in the Look-up Table. When the module completes writing all the Data Words to the block, the module sets this bit to 0. This indicates to write to the even-numbered block the next time receive data comes in for this RTid.
04	Double Buffering (Receive) selected[1]	The bit indicates that the module will double buffer data for the receive messages for this RTid. When the module receives messages for an RTid, the data is stored in the assigned datablock. If no datablock is assigned, data is stored in the default datablock (number 0). When two messages arrive for the same RTid, the data of the second message will overwrite the data of the first message. To preserve the data of the first message long enough to be able to read it before it gets overwritten, use a double buffering scheme to save the data of the last two messages; i.e., use two buffers, alternatively, so that the module can capture data to one buffer, and simultaneously the user can read data from the other buffer. To implement double buffering, the module requires that the datablock assigned to this RTid be an even number. The module then reserves the following odd-numbered block as the paired block for use in double buffering. **Note:** If Double Buffering is enabled for this RTid, and the block number selected is odd, double buffering does not occur. Instead: 1. A flag at Bit 02 in the Message Received Status register is set (see **2.11.12 Message Received Status Register** on page 2-25); 2. The selected (odd) block number is written to the Bad Block Number register (3E92 H) to indicate the error (see **2.11.31 Bad Block Number Register** on page 2-32); 3. The RTid is written to the RTid with Bad Block Number register (3E94 H, see **2.11.30 RTid with Bad Block Number Register** on page 2-32).

RTid Information Word

Bit	Bit Name	Description
03	Inactive[1]	The RTid is inactive – message is not processed at all; the RT does not send back a Status Word. **Note:** RT response time must be set to at least 5 µsec., otherwise there will be extraneous words on the bus.
02	Illegalization	The ME bit (Bit 10) is set in the 1553 RT Status Word (see **2.11.44 1553 RT Status Word Table** on page 2-38). Only the Status Word is sent back. For **BC-to-RT** (receive) messages – processing continues as per regular algorithm, and the ME bit is written in the STW. For **RT-to-BC** (transmit) messages – no data is sent. For **RT-to-RT** messages – receive part: the ME bit is written in the STW; transmit part: no data is sent For **Mode Code** messages – the ME bit is written in the STW **Note:** On a single function module (*PxS*), illegalization is done based on the SAid, not the RTid. See **2.3.2.3 Subaddress Identifier (SAid)** on page 2-10.
01	Interrupt on Error[2]	Generates an interrupt on error
00	Interrupt on end of message[2]	Generates an interrupt on end of message

RTid Information Word (Continued)

1. Not applicable to Mode Codes
2. If the interrupt bit is set in the RT Settings Table, the interrupt setting in the RTid Control Table is ignored. To set an interrupt at the RTid level, make sure the interrupt in the RT Settings Table is disabled.

2.11.8 Module Configuration Register   Address: 3FFF (H)

Use the Module Configuration register to set the operating mode of the module.

Set the Module Configuration register before issuing a Start command to the module. To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24).

Hex Value	Operating Mode
02	RT mode

Module Configuration Register

2.11.9 Module ID Register   Address: 3FFE (H)

The Module ID register contains a fixed value that can be read by the initialization routine to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

2.11.10 Module Status Register — Address: 3FFD (H)

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to '1'.

Bit	Description
07	1 = Always set
05 – 06	Indeterminate
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit in the Start register is cleared. Following this, the module sets Bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic '1'.

2.11.11 Start Register — Address: 3FFC (H)

The Start register controls the Start/Stop operation of the module. The user can Start or Stop the RT operation, modify RT parameters, for example: the Error Injection register or RT Response Time register, and then issue a new Start command in real time.

See also **2.11.10 Module Status Register**, Bit 04 (Module Halted/Running).

Bit	Description
01 – 07	0
00	1 = Start 0 = Stop

Start Register

Note: The user can start the module externally by sending a minimum LVTTL pulse of 100 nsec. to the EXSTARTn pin. See **7.4.2 Module Terminal Stick Pin Assignments** on page 7-4.

2.11.12 Message Received Status Register **Address: 3FFB (H)**

The Message Received Status register indicates that a 1553 message has been received. A logic '1' indicates active condition. This bit is also set for messages with errors.

Bit	Description
01 – 07	0
00	Message Content

Message Received Status Register

Note: After reading, reset the Message Complete bit; the module does not reset this bit.

2.11.13 Time Tag Resolution Register **Address: 3FF7 (H)**

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 μsec.

To determine the Time Tag Counter's resolution, use the following equation:

= (Time Tag Resolution register value + 1) × 4 μsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the module. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.)

2.11.14 Bit Count Register — Address: 3FF6 (H)

The Bit Count register sets the total number of bits in the 1553 Word, including Sync (3) and Parity (1). This register is used by the module only for messages for which the Bit Count Error bit is set in the Error Injection register. (See **2.11.16 Error Injection Register** on page 2-27). If, the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

Set the Bit Count register before issuing a Start command to the module. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.)

Bit	Description			
03 – 07	0			
00 – 02	Bit 02	Bit 01	Bit 00	Number of 1553 bits sent per word
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Count Register

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

2.11.15 RT Response Time Register — Address: 3FF4 (H)

The RT Response Time register sets the Response Time of the remote terminal. The resolution of the Response Time register is 155 nsec. per bit. The minimum time is approximately 4 µsec., which is achieved by writing a 0 to this register. Any value above zero results in:

Response Time = 4 µsec.+ (RT Response Time register x 155 nsec.)

Tolerance of response time: ± 1 µsec.

Set the Response Time register before issuing a Start command to the module. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.)

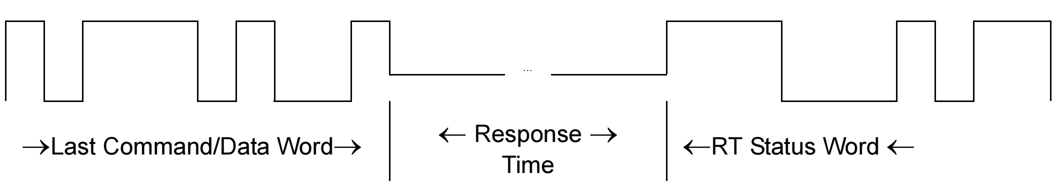


Figure 2-11 RT Response Time Definition

Example: To request a Response time of 9 µsec:
Write 32 to the RT Response Time register
$32 \times 0.155 \cong 5$ µsec + 4 µsec = 9 µsec

2.11.16 Error Injection Register **Address: 3FF3 (H)**

The Error Injection register is a global register that allows the user to select the type of error to be injected in a transmitted message. When the module receives a Start command (issued by writing to the Start register), the module reads this register.

To modify the Error Injection register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24)

Bit	Description
07	Data Word Sync Error (Data Words sent with Command Sync)
06	Data Word Parity Error (Data Words sent with Even Parity)
05	Status Word Synchronization Error (Status Word Sent With Data Sync)
04	Status Word Parity Error (Status Word sent with Even Parity)
03	Reserved – set to 0
02	Non-Contiguous Data (Between First and Second Data Word)
01	Bit Count Error See **2.11.14 Bit Count Register** on page 2-26.
00	Reserved – set to 0

Error Injection Register

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

2.11.17 Variable Amplitude Register **Address: 3FF2 (H)**

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.0 volts (peak-to-peak) when measured on the 1553 bus using Direct Coupling mode and 39-Ohm load (that is, two 78-Ohm termination resistors). The Variable Amplitude register has a resolution of 28 mV/bit (p-p) on the bus.

These values are correct on an ideal system. In practice, the actual signal amplitude can vary approximately ±1 volt (p-p) depending on the characteristics of the system components (cables, connectors, transformers, couplers, etc.). In addition, the more bus connections (bus load) the more the actual amplitude is reduced.

Set the Variable Amplitude register before issuing a Start command to the module. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.) After a reset, the Variable Amplitude register defaults to FF (H), providing maximum amplitude.

Note: On a single function module (*PxS*), the amplitude is not variable and is set to 7.0 volts (p-p).

2.11.18 Old RT Message Stack Pointer — Address: 3FF0 – 3FF1 (H)

The Old RT Message Stack pointer indicates the Old RT Message Stack position. After the entire message is received, the pointer is updated (incremented by 6). This word is initialized to 3300(H) and circulates in the message stack between 3300(H) and 33FB(H). This pointer has been retained for backward compatibility. See **2.5.1 Old RT Message Stack** on page 2-13.

For information on the current RT Message Stack pointer, see **2.11.25 RT Message Stack Pointer** on page 2-31.

2.11.19 RT Protocol Options Register — Address: 3FEF (H)

Bit 02 of the RT Protocol Options register is used to select which message stacks to use.

Bit 01 of the RT Protocol Options register is used to select a 1553 environment: MIL-STD-1553A or MIL-STD-1553B.

Depending on the 1553 environment selected, certain bits in the 1553 RT Status Word will be affected. See **2.11.44 1553 RT Status Word Table** on page 2-38.

Bit 00 of the register is used to set the Status Response (Suppress or Send status) mode of operation.

If set to 'send' after a Receive message, the RT will can respond with a 1553 Status Word even if an invalid 1553 Data Word was received.

To define Mode Codes as SA-31 and process as 1553A compatible, see **2.11.42 Mode Code Control Register** on page 2-37.

The RT Protocol Option register must be set before issuing a Start command to the module. To modify the RT Protocol Option register, issue a Stop command, modify the register, then, issue a Start command. (See **2.11.11 Start Register** on page 2-24).

Bit	Description	
03 – 07	0	
02	Message Stack	0 = (**Default**) Only the new message stack is available, 512 blocks 1 = Both message stacks are available; new (512 blocks) and old (42 blocks) See **2.2 RT Memory Map** on page 2-4 for addresses.
01	Environment	0 = 1553B 1 = 1553A Mode Code compatibility Mode Codes are user-defined (except for MC-0), subaddresses are set to 0, no Data Words. RT sends back a Status Word only.
00	On Error	0 = Suppress Status 1 = Send Status

Status Response Register

2.11.20 Module Function Register

Address: 3FEA – 3FEB (H)

Set Bit 00 of the Module Function register to 1 to enable Expanded Block mode. Expanded Block mode increases the available block numbers to 511, and reduces the Internal Concurrent Monitor from 409 to 204 messages.

2.11.21 Broadcast Control Register

Address: 3FE8 – 3FE9 (H)

Set the Broadcast Control register to specify whether RT address 11111 (RT #31) should be regarded as a valid RT number or as the Broadcast address.

In Broadcast mode, the module stores the received message in a 1553 Data Block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block Look-up Table memory.

Note:

- When operating in Broadcast mode, the active RT Look-up Table entry must be set for RT#31 as Not Active.
- This register replaces the use of Bit 00 of the Options Select register. See **2.11.4 Options Select Register** on page 2-19.

Bit	Description
01 – 15	0
00	1 = RT #31 is Broadcast Address 0 = RT #31 is Regular RT

Broadcast Control Register

2.11.22 1760 Header Value Transmit Table **Address: 3F40 – 3F7F H**

1760 Option only

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message. If the wrong data was sent, the Internal Concurrent Monitor will set an error bit. See Bit 06 in the **Message Status Word: RT/ Internal Concurrent Monitor** on page 5-3.

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

SA #31 1760 Header Value Transmit Word	3F7E H
• • •	• • •
SA #1 1760 Header Value Transmit Word	3F42 H
SA #0 1760 Header Value Transmit Word	3F40 H

Figure 2-12 1760 Header Value Transmit Table

Transmit Subaddress	Header Value	Address
1	**0421 H**	3F42 H
11	**0420 H**	3F56 H
14	**0423 H**	3F5C H

Predefined 1760 Transmit Header Values

2.11.23 1760 Header Value Receive Table **Address: 3F00 – 3F3F (H)**

1760 Option only

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. The module checks that the specified Header receive value was received. In addition, the Internal Concurrent monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header Error** bit is set in the Message Status Word. See **2.5.2 Message Status Word** on page 2-14.

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

SA #31 1760 Header Value Receive Word	3F3E H
• • •	• • •
SA #1 1760 Header Value Receive Word	3F02 H
SA #0 1760 Header Value Receive Word	3F00 H

Figure 2-13 1760 Header Value Receive Table

Receive Subaddress	Header Value	Address
11	**0400 H**	3F16 H
14	**0422 H**	3F1C H

Predefined 1760 Receive Header Values

2.11.24 1760 Header Exist Table **Address: 3EC0 – 3EFF (H)**

1760 Option only

The 1760 Header Exist Table contains 32 entries corresponding to 32 Subaddresses. Each entry may be set to indicate whether the module should expect a Header word for BC-to-RT or RT-to-RT messages directed to that subaddress.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on each module.

To set other values, enable the Header Exist Table entry for this Subaddress (set it to 1) and write the value to the Header Value (Transmit/Receive) Table.

SA #31 1760 Header Exist Word	3EFE H
⋮	⋮
SA #1 1760 Header Exist Word	3EC2 H
SA #0 1760 Header Exist Word	3EC0 H

Figure 2-14 1760 Header Exist Table

Bit	Description
09-15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC or RT-to-RT) 0 = Module should **not** expect a Header word in a transmit message
01 – 07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should **not** expect a Header word in a receive message

1760 Header Exist Table

Associated Subaddress	Header Value	Address
1	**0100 H**	3EC2 H
11	**0101 H**	3ED6 H
14	**0101 H**	3EDC H

Predefined 1760 Headers

2.11.25 RT Message Stack Pointer **Address: 3EBE – 3EBF (H)**

The RT Message Stack pointer indicates the next word to be written to the RT message stack. After the entire message is received, the message stack pointer is updated (incremented by 8). This word is initialized to 6000 (H) and circulates in the message stack between 6000(H) and 6FFF(H).

2.11.26 Module Time Register Lo & Hi

Address: 3EA4 – 3EA5 (H)
3EA2 – 3EA3 (H)

This register holds the module time value, which is stored in non-volatile flash memory and loaded at power-up. This value can be modified by calling the Set_ModuleTime_Px function. (See the *1553Px Family Software Tools Programmer's Reference*.) The factory default value is FFFF FFFF (H).

2.11.27 Serial Number Register

Address: 3EA0 – 3EA1 (H)

This register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660.

2.11.28 Error Counter Lo & Hi

Address: 3E9E – 3E9F (H)
3E9C – 3E9D (H)

Error Counter is a running 32-bit counter of message errors.

2.11.29 Message Counter Lo & Hi

Address: 3E9A – 3E9B (H)
3E98 – 3E99 (H)

Message Counter is a running 32-bit counter of all messages received.

2.11.30 RTid with Bad Block Number Register

Address: 3E94 – 3E95 (H)

When using double-buffering, odd-numbered block numbers are invalid. The RTid with Bad Block Number register indicates the associated RTid for which the user attempted to set an odd-numbered block when using double-buffering.

2.11.31 Bad Block Number Register

Address: 3E92 – 3E93 (H)

When using double-buffering, odd-numbered block numbers are invalid. The Bad Block Number register indicates the selected invalid odd-numbered block.

2.11.32 Clear Time Tag on Sync Register

Address: 3E88 – 3E89 (H)

Write 1 to the lower byte (3E88 H) of the Clear Time Tag on Sync register to indicate that the module should clear the Time Tag counter (7008 – 700B H) (resets to 0) upon receipt of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Write 1 to the higher byte (3E89 H) of the Clear Time Tag on Sync register to indicate that the module should clear the Time Tag counter (7008 – 700B H) (resets to 0) upon receipt of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

Note: This register setting does not take effect until the module is restarted.

2.11.33 More Module Options Register — Address: 3E86 – 3E87 (H)

Read only The More Module Options register is a 16-bit register that provides additional module information.

Bit	Description
06 – 15	Reserved
05	1 = Expanded Block mode is available in BC mode 0 = Expanded Block mode is not available in BC mode
04	1 = Enhanced Monitor mode is available in Sequential Fixed-Block Monitor mode 0 = Enhanced Monitor mode is not available in Sequential Fixed-Block Monitor mode
03	1 = Expanded Block mode is available in Sequential Fixed-Block Monitor mode 0 = Expanded Block mode is not available in Sequential Fixed-Block Monitor mode
02	1 = Module is single function (*PxS*) 0 = Module is multifunction (*Px*)
01	1 = Onboard Loopback option is available 0 = Onboard Loopback option is not available
00	1 = Module is only available in Monitor mode 0 = Module is available in all modes

More Module Options Register

2.11.34 Module Options Register — Address: 3E84 – 3E85 (H)

Read only The Module Options register is a 16-bit register that provides information about the internal processor and firmware.

Bit	Description
15	1 = PxIII
14	Reserved; set to 1
13	1 = Expanded Block mode is in use in RT mode
12	1 = Module is on a removable card (PCMCIA or ExpressCard) 0 = Module is on an add-in board
11	1 = Replay mode is in use (BC mode only)
10	1 = PxII
09	1 = 1760
08	1 = 1553
00 – 07	4D H Always set; indicates Internal Concurrent Monitor

Module Options Register

2.11.35 Firmware Revision Register Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-module firmware. The value 18 (H) would read as revision level '1.8'.

2.11.36 1553 RT Vector Word Table Address: 3480 – 34BF (H)

The RT Vector Word locations are reserved for the 32 1553 Vector words. (On a single function module (*PxS*), only one word is used at 3480 H and the rest is reserved.) Load the desired Vector words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used to implement the Transmit Vector Word Mode Code.

RT #31 1553 RT Vector Word	34BE H
⋮	⋮
RT #1 1553 RT Vector Word	3482 H
RT #0 1553 RT Vector Word	3480 H

Figure 2-15 1553 RT Vector Word Table

Note: For a description of the BC's reaction to the SRQ bit and the Vector Word, see, **3.10 Service Request (SRQ) Processing** on page 3-16.

2.11.37 1553 RT BIT Word Table Address: 3440 – 347F (H)

The RT BIT (Built-in Test) word locations are reserved for the 32 1553 BIT words. (On a single function module (*PxS*), only one word is used at 3440 H and the rest is reserved.) Load the desired BIT words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used to implement the Transmit BIT Word Mode Code.

RT #31 1553 RT BIT Word	347E H
⋮	⋮
RT #1 1553 RT BIT Word	3442 H
RT #0 1553 RT BIT Word	3440 H

Figure 2-16 1553 RT BIT Word Table

2.11.38 RT Last Command Word Table **Address: 3400 – 343F (H)**

The Last Command Word locations are reserved for the 32 1553 Last Command Words. (On a single function module (*PxS*), only one word is used at 3400 H and the rest is reserved.) The module writes to these locations at the end of each message transfer (for active RTs only). The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used for the implementation of the Transmit Last Command Word Mode Code.

Note: Only Command Words of valid messages containing no errors are recorded in this table.

RT #31 Last Command Word	343E H
• • •	• • •
RT #1 Last Command Word	3402 H
RT #0 Last Command Word	3400 H

Figure 2-17 RT Last Command Word Table

2.11.39 Interrupt Condition Register **Address: 33FC (H)**

The Interrupt Condition register allows the user to enable an interrupt trigger. The bits work in conjunction with the Interrupt bit in the RT Settings Table. When a message is received by an RT for which the Active RT interrupt bit is set, the module will check the Interrupt Condition register.

If the module has completed receiving the Command Word and the Begin Data bit is also set, an interrupt trigger will be generated.

If the module has completed processing the message and the Message Complete bit is also set, an interrupt trigger will be generated.

Set the Interrupt Condition register before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.)

Bit	Description
02 – 07	0
01	1 = Message Complete
00	1 = Begin Data

Interrupt Condition Register

2.11.40 Old RT Message Stack — Address: 3300 – 33FB H

This message stack has been retained for backward compatibility. For more information, see **2.5.1 Old RT Message Stack** on page 2-13.

2.11.41 Word Count Error Table — Address: 32E0 – 32FF (H)

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per Remote Terminal). The first byte is for RT#0, the second to RT#1, and the last byte is for RT#31. The contents of each location controls the number of 1553 Words (±3 words) in the message. The variation is an offset, relative to the 1553 Command Word's Word Count field. The resulting message (if an error is programmed) must contain at least one Data Word.

Upon power-up and software reset, the module sets the Word Count Error Table to the default value, 0.

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

The user must set the Word Count Error register before issuing a Start command to the module. To modify the Word Count Error register, issue a Stop command, modify the register, and then issue a Start command. See **2.11.11 Start Register** on page 2-24.

RT #31 Word Count Error Byte	32FF H
⋮	⋮
RT #1 Word Count Error Byte	32E1 H
RT #0 Word Count Error Byte	32E0 H

Figure 2-18 Word Count Error Table

Register Value	Word Count Offset
FD H	-3 Words
FE H	-2 Words
FF H	-1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Error Byte Values

2.11.42 Mode Code Control Register

Address: 3266 (H)

The Mode Code Control register allows the user to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command to the module. To modify the Mode Code Control register, issue a Stop command, modify the register, and then issue a Start command. (See **2.11.11 Start Register** on page 2-24.)

Bit	Description		
02 – 07	0		
00 – 01	**Bit 01**	**Bit 00**	**Subaddresses recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

2.11.43 1760 Checksum Limits Register

Address: 3264 – 3265 (H)

1760 Option only

Write a value to the 1760 Checksum Limits register to set the Data Blocks for which the module should calculate a checksum value. The module will calculate a checksum value for those Data Blocks whose numerical index is less than the value stored in this register. Maximum value is 256 (512 when using Expanded Block mode).

Example: Write 20 to the Checksum Limits register when you want Data Blocks 0 – 19 to have a checksum value. This causes the module to:

1. Transmit a checksum value as the last word in the Data Block (transmit message).
2. Check the last word in the Data Block for a checksum value (receive message).

2.11.44 1553 RT Status Word Table **Address: 3220 – 325F H**

These locations (3220 – 325F H) are reserved for the 32 1553 RT Status Words. (On a single function module (*PxS*), only one word is used at 3220 H and the rest is reserved.) Load the desired Status Words into their respective locations in the block. The first word relates to RT#0, the next word to RT#1, while the last word relates to RT#31.

Whenever the RT has to respond with a Status Word, the module sends out the Status Word as the user has defined it with the addition of certain other bits that the module may set, as described below.

The user may set the RT Status Word for one-time use only. See Bit 04 of the RT Settings Table (see **2.4 RT Settings Table** on page 2-10). If Duration is set to 1 ('one-time'), the RT Status Word user-defined bits (bits 00 – 10) will be used only once, then cleared and set by the module according to the rules described below. The top 5 bits, i.e. the RT Address Field remain unchanged.

Note: If an error occurred in the Command Word, the module cannot send out an RT Status Word – the RT is unknown.

RT #31 1553 RT Status Word	325E H
⋮	⋮
RT #1 1553 RT Status Word	3222 H
RT #0 1553 RT Status Word	3220 H

Figure 2-19 1553 RT Status Word Table

2.11.44.1 RT Status Word Bits

In both MIL-STD-1553A and MIL-STD-1553B environments bits 11 – 15 are the RT Address Field and Bit 10 is the Message Error bit. Bits 00 – 09 are reserved in a 1553A environment but in a 1553B environment apply as shown in the following table.

Bit	MIL-STD-1553A	MIL-STD-1553B	Description
11 – 15	RT Address	RT Address	
10	Message Error	Message Error	Invalid or illegal word/s received in preceding command
09	Reserved	Instrumentation	Always 0, to distinguish between cmd and status
08	Reserved	Service Request (SRQ)	Indicates to BC that RT needs servicing
05 – 07	Reserved	Reserved	
04	Reserved	Broadcast	Preceding Command Word was a broadcast command
03	Reserved	Busy	RT cannot send data in response to BC command
02	Reserved	Subsystem Flag	RT fault exists; data being requested may be invalid
01	Reserved	Dynamic Bus	Acceptance of offer by active BC to be the next BC
00	Reserved	Terminal Flag	RT fault condition (used with Mode Codes 6,7,19)

1553A and 1553B RT Status Word Bits

The 1553 environment, 1553A or 1553B, is set by the user in the RT Protocol Options register. See **2.11.19 RT Protocol Options Register** on page 2-28.

Message Error Bit (Bit 10)

If the message is of type Send Status (see **2.11.19 RT Protocol Options Register** on page 2-28), and an error occurred in the data of a message, the module will set the Message Error (ME) bit in the Status Word to 1 prior to sending it out.

If the message is of type Suppress Status, and an error occurred in the data of a message, the module will not send out a Status Word at all. But, on the next message, the module will send out the Status Word with the ME bit set to 1. The ME bit will be reset to the user-defined value when the next valid command is received by the RT (unless the next valid command is Mode Code Transmit Status Word or Mode Code Transmit Last Command).

If the RTid has been set illegal by the user, the module will always set the ME bit to 1 in the Status Word sent back in response to a command for that RTid, whether the message is of type Send or Suppress Status.

Service Request BIT (SRQ – Bit 08)

Setting the SRQ bit indicates to the BC that a subaddress on this RT requires servicing. (For BC processing of this bit, see **3.10 Service Request (SRQ) Processing** on page 3-16).

Note: Simulated RTs do not support SRQ processing.

Broadcast (Bit 04)

If a Broadcast message is received, the module does not send out a Status Word. But, each active RT, on the next message it receives, will send out the Status Word with the Broadcast Bit set to 1. (In a Broadcast RT-to-RT, the transmitting RT, even if active, will never have the broadcast bit set).

The Broadcast Bit will be reset (to the user-defined value) when the next valid command is received by the RT (unless the next valid command is Mode Code Transmit Status Word or Mode Code Transmit Last Command).

Busy (Bit 03)

In the case of Transmit commands, when the user has set the Busy bit, no Data Word will be transmitted by the RT following the transmission of the Status Word.

2.11.45 RT Settings Table   Address: 3200 – 321F H

The RT Settings Table is described earlier in this chapter. See **2.4 RT Settings Table** on page 2-10.

3 BC/Concurrent-RT Operation

Chapter 3 describes module operation in Bus Controller/Concurrent-RT mode. The topics included are:

3.1 BC/Concurrent-RT Mode Overview

Each module can simultaneously operate as the Bus Controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In BC/Concurrent-RT mode, load message blocks with the RT's 1553 Status and Data Words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the 1553 Words appear on the 1553 bus.

Note: The requirement for loading the message blocks only applies to RTs that the user is actively simulating. For inactive RTs (not simulated by the module), leave the corresponding locations blank in the associated 1553 message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 μsec.

To determine if the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module **ID Register** (test for value = 45 H).
2. Check the Module **Status Register** (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values. For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a '1' to the Start register is referred to as issuing a Start command.

3.2 BC/Concurrent-RT Memory Map

The following memory maps show the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

Internal Concurrent Monitor Message Block Area[1]	8000 – FFFF H
Instruction Stack / Message Block Area	7100 – 7FFF H
Reserved	700C – 70FF H
Time Tag (Hi)	700A – 700B H
Time Tag (Lo)	7008 – 7009 H
Time Tag Reset Register	7007 H
Reserved	7004 – 7006 H
Loopback Relay Select Register	7003
Reserved	7001 – 7002 H
Module Reset Register	7000 H
Instruction Stack /Message Block Area	4000 – 6FFF H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
RT Response Time Register	3FF9 H
Reserved	3FF7 – 3FF8 H
Loop Count Register	3FF6 H
Bit Error Register	3FF5 H
Word Count Register	3FF4 H
BC Response Time Register	3FF3 H
Variable Amplitude Register[3]	3FF2 H
Message Stack Pointer	3FF0 – 3FF1 H
Frame Time Multiplier Register	3FEE – 3FEF H
Frame Time Resolution Register	3FEC – 3FED H
Instruction Counter	3FEA – 3FEB H
Minor Frame Time Register	3FE8 – 3FE9 H
Minor Frame Time Multiplier Register	3FE6 – 3FE7 H
Replay Register	3FE4 – 3FE5 H
Reserved	3FDE – 3FE3 H
Zero Cross Bit Index Register	3FDC – 3FDDH
Error Word Index Register	3FDA – 3FDB H
Sync Pattern Register	3FD8 – 3FD9 H

Reserved	3FD4 – 3FD7 H
SRQ Counter	3FD2 – 3FD3 H
SRQ Message Status Register	3FCE – 3FD1 H
SRQ Message 2 Register	3F88 – 3FCD H
SRQ Message 1 Register	3F80 – 3F87 H
1760 Header Value Transmit Table[2]	3F40 – 3F7F H
1760 Header Value Receive Table[2]	3F00 – 3F3F H
1760 Header Exist Table[2]	3EC0 – 3EFF H
Reserved	3EA6 – 3EBF H
Module Time Register (Lo)	3EA4 – 3EA5 H
Module Time Register (Hi)	3EA2 – 3EA3 H
Serial Number Register	3EA0 – 3EA1 H
Error Counter (Lo)	3E9E – 3E9F H
Error Counter (Hi)	3E9C – 3E9D H
Message Counter (Lo)	3E9A – 3E9B H
Message Counter (Hi)	3E98 – 3E99 H
Reserved	3E92 – 3E97 H
Internal Concurrent Monitor Next Message Pointer[1]	3E90 – 3E91 H
Module Function Register	3E8E – 3E8F H
BC Protocol Options Register	3E8C – 3E8D H
Send Time Tag on Sync Register	3E8A – 3E8B H
Clear Time Tag on Sync Register	3E88 – 3E89 H
More Module Options Register	3E86 – 3E87 H
Module Options Register	3E84 – 3E85 H
Reserved	3E81 – 3E83 H
Firmware Revision Register	3E80 H
Reserved	3426 – 3E7F H
Asynchronous Start Flag	3424 – 3425 H
Asynchronous Frame Pointer Register	3422 – 3423 H
Asynchronous Message Count Register	3420 – 3421 H
RT Settings Table	3400 – 341F H
Instruction Stack /Message Block Area	0000 – 33FF H

Figure 3-1 BC/Concurrent-RT Memory Map for PCI[e] Carrier Boards

1. See **Chapter 5: Internal Concurrent Monitor**
2. 1760 Option only
3. On a single function module (*PxS*) this register is reserved

Internal Concurrent Monitor Message Block Area[1]	8000 – FFFF H		
Instruction Stack /Message Block Area	7100 – 7FFF H	Error Word Index Register	3FDA – 3FDB H
Reserved	700C – 70FF H	Sync Pattern Register	3FD8 – 3FD9 H
Time Tag (Hi)	700A – 700B H	Reserved	3FD4 – 3FD7 H
Time Tag (Lo)	7008 – 7009 H	SRQ Counter	3FD2 – 3FD3 H
Reserved	7007 H	SRQ Message Status Register	3FCE – 3FD1 H
Time Tag Reset Register	7006 H	SRQ Message 2 Register	3F88 – 3FCD H
Reserved	7003 – 7005 H	SRQ Message 1 Register	3F80 – 3F87 H
Loopback Relay Select Register	7002 H	1760 Header Value Transmit Table[2]	3F40 – 3F7F H
Module Reset Register	7001 H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Reserved	7000 H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Instruction Stack /Message Block Area	4000 – 6FFF H	Reserved	3EA6 – 3EBF H
Module ID Register	3FFF H	Module Time Register (Lo)	3EA4 – 3EA5 H
Module Configuration Register	3FFE H	Module Time Register (Hi)	3EA2 – 3EA3 H
Start Register	3FFD H	Serial Number Register	3EA0 – 3EA1 H
Module Status Register	3FFC H	Error Counter (Lo)	3E9E – 3E9F H
Message Status Register	3FFB H	Error Counter (Hi)	3E9C – 3E9D H
Interrupt Condition Register	3FFA H	Message Counter (Lo)	3E9A – 3E9B H
Reserved	3FF9 H	Message Counter (Hi)	3E98 – 3E99 H
RT Response Time Register	3FF8 H	Reserved	3E92 – 3E97 H
Loop Count Register	3FF7 H	Internal Concurrent Monitor Next Message Pointer[1]	3E90 – 3E91 H
Reserved	3FF6 H	Module Function Register	3E8E – 3E8F H
Word Count Register	3FF5 H	BC Protocol Options Register	3E8C – 3E8D H
Bit Error Register	3FF4 H	Send Time Tag on Sync Register	3E8A – 3E8B H
Variable Amplitude Register[3]	3FF3 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
BC Response Time Register	3FF2 H	More Module Options Register	3E86 – 3E87 H
Message Stack Pointer	3FF0 – 3FF1 H	Module Options Register	3E84 – 3E85 H
Frame Time Multiplier Register	3FEE – 3FEF H	Reserved	3E82 – 3E83 H
Frame Time Resolution Register	3FEC – 3FED H	Firmware Revision Register	3E81 H
Instruction Counter	3FEA – 3FEB H	Reserved	3426 – 3E80 H
Minor Frame Time Register	3FE8 – 3FE9 H	Asynchronous Start Flag	3424 – 3425 H
Minor Frame Time Multiplier Register	3FE6 – 3FE7 H	Asynchronous Frame Pointer Register	3422 – 3423 H
Replay Register	3FE4 – 3FE5 H	Asynchronous Message Count Register	3420 – 3421 H
Reserved	3FDE – 3FE3 H	RT Settings Table	3400 – 341F H
Zero Cross Bit Index Register	3FDC – 3FDDH	Instruction Stack /Message Block Area	0000 – 33FF H

Figure 3-2 BC/Concurrent-RT Memory Map for VME/VXI Carrier Boards

1. See **Chapter 5: Internal Concurrent Monitor**
2. 1760 Option only
3. On a single function module (*PxS*) this register is reserved

3.3 Instruction Stack

The Instruction Stack is used to program the module. The stack is divided into instruction blocks, each containing four words. The block contains control information (that the user writes) and status information (that the module writes).

Figure 3-3 Instruction Block Structure – BC/Concurrent-RT Mode illustrates one instruction block.

Control and status information is stored in the memory in the following sequence:	Byte Offset
Message Status Word	+6
Intermessage Gap Time Counter	+4
Intermessage Gap Time	+2
Message Block Pointer	0

Figure 3-3 Instruction Block Structure – BC/Concurrent-RT Mode

3.3.1 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the RT 1553 Status Word. (See **2.4 1553 RT Status Word** on page 2-7). The contents of the Message Status Word are described below.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed
14	**Checksum Error** (1760 Option only)	The calculated checksum (on an incoming message) does not match the last Data Word received. See **3.11.2 Checksum** on page 3-17.
13	**Incorrect 1553 Channel**	Remote Terminal response was not received on the active 1553 module.
12	**Message Error Bit**	Message Error bit (Bit 10) in the RT Status Word was set.
11	**RT Status Bit**	A bit was set in the RT Status Word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A 1553 message-level error occurred (e.g. Word Count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late – see **3.13.16 BC Response Time Register** on page 3-26.
08	**1760 Header Word** (1760 Option only)	Header Word received does not match the value set in the Header Value Table. See **3.11.1 Header Word** on page 3-17.
07	**Invalid Word Received**	At least one invalid 1553 Word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Lo**	RT transmitted too few words.
04	**Incorrect RT Address**	1553 Status Word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the status or Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 Words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. The error type is defined in one of the other message status bit locations.

Message Status Word

Note:

- A logic 1 indicates occurrence of status flag.
- The Message Status Word is valid only when Bit 15, End of Message, is turned on.
- To ensure data integrity, the module sets a special status value of 7F00 H (NO_ALTER) to indicate that a message is currently being transmitted or received. Check this value before attempting to change the Data words of the message.

3.3.2 Intermessage Gap Time

The Intermessage Gap Time (IGT) value is a 16-bit word that the user writes, that allows a unique intermessage delay time to be inserted between the current message and the next message. The minimum IGT is approximately 8 μsec. The maximum IGT is approximately 10 msec. that can be extended up to approximately 80 seconds, using the IGT counter value. (See **3.3.3 Intermessage Gap Time Counter/Message Function Select** on page 3-7.) The value in the word is added to this minimum time. The resolution of this word is 155 nsec. per bit.

3.3.3 Intermessage Gap Time Counter/Message Function Select

The 13 low bits are the Intermessage Gap Time counter (IGT_counter). It is written by the user, allowing to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used.

The 3 high bits are used to select functionality for the message.

Bit 13 is used to instruct the module to generate an interrupt when the specific message is completed.

The user sets bits 14 and 15 to instruct the module to generate checksums and checksum error detection and injection. See **3.11.2 Checksum** on page 3-17.

Bit	Bit Name	Description
15	**Chk_Sum_On** (1760 option only)	BC-to-RT: Generate a checksum *or* RT-to-BC: Checks that the correct Checksum was transmitted
14	**Chk_Sum_Err_Inj** (1760 option only)	BC-to-RT message: Injects an incorrect value into the checksum; Bit 15 must be set in order to set Chk_Sum_Err_Inj **Note:** On a single function module (*PxS*) this bit is reserved. Error injection is not available.
13	**Int_On_Select_Msg**	1 = Generate an interrupt when this specific message is completed. To set general interrupt conditions. See **3.13.10 Interrupt Condition Register** on page 3-22
00 – 12	**IGT_counter**	Write a value to increase the IGT by repeating the number of times the IGT value is used. For example, if the counter is set to 0, then the gap time is not repeated; and depends on the contents of the IGT location. If the gap time counter is 1, then the gap time is repeated once and equals the IGT value × 2, etc. **Note:** To ensure maximum IGT accuracy when using the IGT_counter, use the largest possible value for the IGT word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

Intermessage Gap Time Counter

3.3.4 Message Block Pointer

The Message Block pointer is a 16-bit word that the user writes to point to the beginning of a 1553 message block.

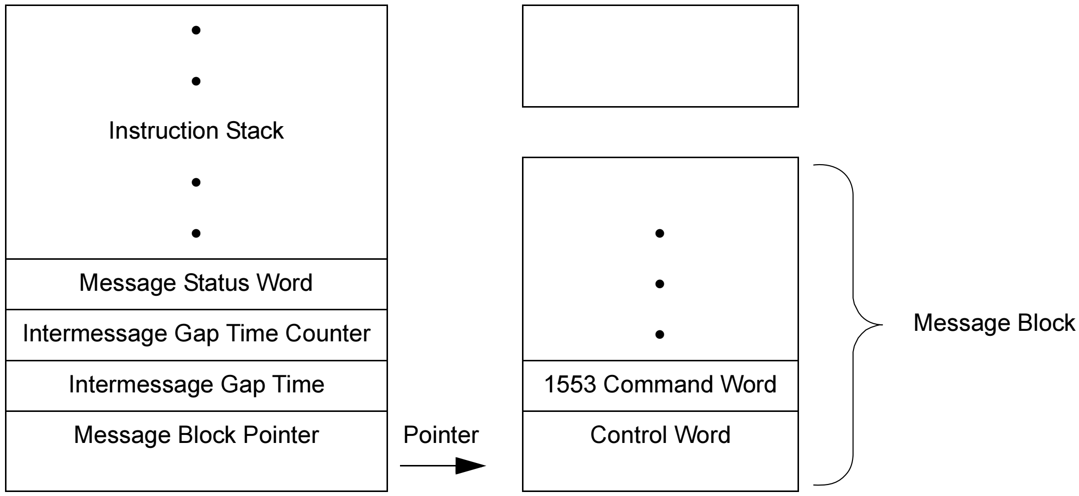


Figure 3-4 Message Block Pointer – BC/Concurrent-RT Mode

3.4 Message Block

The message block can be loaded anywhere in the Instruction Stack/Message Block area. (See **Figure 3-1 BC/Concurrent-RT Memory Map for PCI[e] Carrier Boards** on page 3-3.) Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers point to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the module which type of message to transmit (i.e., RT-to-RT, Mode Code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC-to-RT, RT-to-BC and RT-to-RT) are illustrated in section **3.4.1 Message Block Formats** on page 3-9.

For a description of each bit see **3.4.2 Control Word** on page 3-11.

3.4.1 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command Word(s), Data Word(s), and Status Word(s). Examples of Message block formats are:

Example No. 1: Transmit Command Operating as BC Only

Block *before* execution

1553 Transmit Command	
Control Word	First Location in Block

Block after execution

1553 Data Word	First Transmitting Remote Terminal (not simulated)
•	•
•	•
1553 Data Word	•
RT Status Word	First Transmitting Remote Terminal (not simulated)
1553 Transmit Command	
Control Word	First Location in Block

Example No. 2: Receive Command Operating as Both BC and Receiving RT

Block *before* execution

RT Status Word	Simulated by *M4K1553Px* (Loaded by user)
1553 Data Word	•
•	•
•	•
1553 Data Word	Simulated by *M4K1553Px* (Loaded by user)
1553 Receive Command	
Control Word	First Location in Block

Block *after* execution

RT Status Word	
1553 Data Word	
•	
•	
1553 Data Word	
1553 Receive Command	
Control Word	First Location in Block

Example No. 3: RT-to-RT Command Operating as BC and Receiving RT

Block before execution

(Receive) RT Status Word	Simulated by *M4K1553Px* (Loaded by user)
Leave empty for Data +N	
•	
•	
Leave empty for Data #1	
Leave empty for (transmit) RT Status Word	
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location in Block

Block after execution

(Receive) RT Status Word	
1553 Data Word	From transmitting Remote Terminal (not simulated)
•	•
•	•
1553 Data Word	•
(Transmit) RT Status Word	From transmitting Remote Terminal (not simulated)
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location in Block

Figure 3-5 Message Block Formats

3.4.2 Control Word

Logic 1 enables the function, 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. Restart by writing to the Instruction Counter register and issue a Start command.
14	**Parity Error**	Selects Even parity in 1553 Word. Also set Bit 08
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. 0 = Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field. (See **3.13.15 Word Count Register** on page 3-26. This function is valid for BC-to-RT messages only.)
11	**Bit Errors**	Transmits invalid number of bits or invalid Zero Cross bit in 1553 Words. (See **2.11.14 Bit Count Register** on page 2-26.)
10	**Incorrect Sync**	Transmits incorrect Sync. Data type Sync is transmitted in the Command Word. Also set Bit 08
09	**Non-Contiguous Data**	Transmits the first 1553 Data Word with an invalid Gap Time (between Command and Data Word). Also set Bit 08
08	**Error Placement/ Error Injection Enable**	Bit 08 applies to Parity, Sync and Bit Count error injection placement for BC-to-RT, Broadcast Receive, and Mode Code receive with Data messages: 0 = Inject error in Command Word 1 = Inject error in Data Words **Note:** • For other message types 0 = Disable error injection 1 = Enable error injection • For Word Count Error. WCerror needs only Bit 12 to be set. The firmware does not look at Bit 08.
07	**Bus A/B**	Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B.
06	**Auto Bus Switch**	On error, the BC will retry message transfer on alternate bus Auto-retry must be selected
04 – 05	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	Bit 04	Description
0	0	No Retries
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00 – 03 Command Code

03	02	01	00	Description
0	0	0	0	Transmit Command (RT to BC)
0	0	0	1	Receive Command (BC to RT)
0	0	1	0	RT-to-RT Command
0	0	1	1	Mode Code
0	1	0	0	Broadcast Receive Command
0	1	0	1	Broadcast RT-to-RT Command
0	1	1	0	Broadcast Mode Code
0	1	1	1	Skip Message [1]
1	0	0	0	Jump Command [2]
1	1	1	1	Minor Frame Command [3]

BC/Concurrent-RT Control Word

1. See **3.4.4 Skip Message** on page 3-12
2. See **3.4.5 Jump Command Operation** on page 3-12
3. See **3.5 Minor Frame Operation** on page 3-13

3.4.3 Halt Operation

Normally set the Halt Operation bit to logic 0 before writing to the Start register. In realtime (during BC execution), the user sets this bit to logic 1. When operating on that particular message block's Control word, the module will halt transfer operations until the bit is reset to logic 0.

When the module detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register. (See **3.13.11 Message Status Register** on page 3-23.) Use the Wait For Continue bit to find out when the module has arrived at the halted instruction block. When the module detects that the Halt bit (Continue mode) has been reset, the module will reset the Wait For Continue bit in the Message Status register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* yet been executed by the module.

Note: The Halt operation can be used in conjunction with the Jump command. See **3.4.5 Jump Command Operation** on page 3-12.

3.4.4 Skip Message

The Skip Message command allows the user to skip a message defined in a certain message block. To do so, modify the Command field in the Control Word. This lets the user selectively send a message in the current frame. The 'skip' takes place immediately and does not wait until the Intermessage Gap Time expires.

3.4.5 Jump Command Operation

The module's BC transfer cycle can be modified by setting the Jump command in the BC Control word. The Jump command instructs the module to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 Command Word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the module has tested the Halt/Continue bit in the Control word. The 'jump' takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated below.

15 ... 8 (High Byte)	7 ... 0 (Low Byte)	
Don't Care	Instruction Count	Third Word
Stack Pointer		Second Word
Control Word		First Word

Figure 3-6 Jump Command Message Block Structure

3.5 Minor Frame Operation

The Minor Frame type of message can be used in the following ways:

- To function as a "delay time" between groups of messages.
- To produce a list of messages that will be sent out over the bus at different frequencies.

Minor frame time is defined as the time elapsed from the beginning of a minor frame to beginning of the next minor frame. To set up minor frame operation, each minor frame must begin with a minor frame command. (See **3.13.22 Minor Frame Time Register** and **3.13.23 Minor Frame Time Multiplier Register** on page 3-29.) The maximum value possible for the Minor Frame Time is 800 milliseconds.

Example: **Figure 3-7 Minor Frame Sequencing** shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

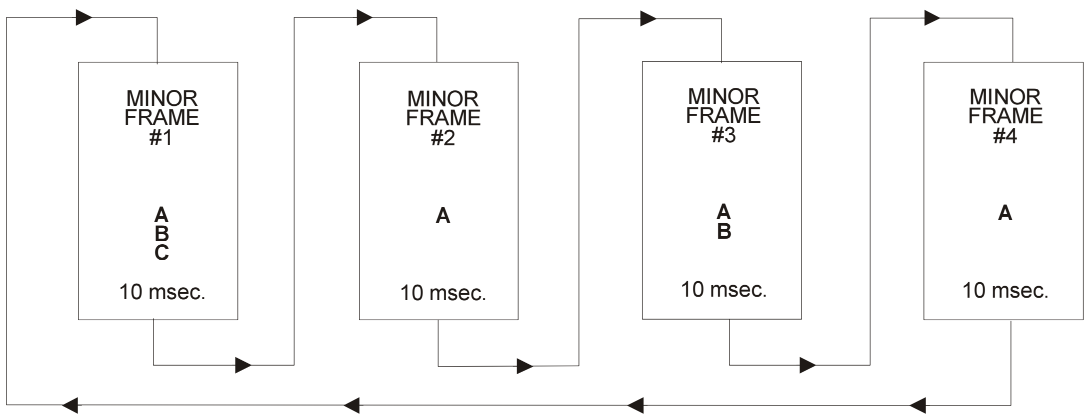


Figure 3-7 Minor Frame Sequencing

Notes:

1. The MINOR_FRAME message does not appear as a real message on the data bus.
2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence. (See **3.13.23 Frame Time Multiplier Register** on page 3-28.)

3.6 Asynchronous Frame Operation

During standard operation, the module sets up a frame of messages and then sends them out synchronously over the bus. The user can set up multiple frames of messages, and select which one to send out.

Asynchronous Frame operation allows the user to transmit a frame asynchronously. This means that in the middle of the transmission of the messages of a frame (frame 1), another frame (frame 2) can be transmitted, and then the module returns to continue transmitting the messages of the original (or synchronous) frame (frame 1).

To transmit an asynchronous frame, the user must write the number of messages in the asynchronous frame into the Asynchronous Message Count register, place a pointer to the beginning of the asynchronous frame in the Asynchronous Frame Pointer register, and then set the Asynchronous Start Flag register to a non-zero value. This will send out the asynchronous frame over the bus. (See **3.13.46 Asynchronous Start Flag Register**, **3.13.47 Asynchronous Frame Pointer Register** and **3.13.48 Asynchronous Message Count Register** on page 3-36.)

3.7 Remote Terminal Simulation

Not for single function module (*PxS*)

When the module is simulating both the Bus Controller and one or more Remote Terminals, the user must write the simulated Remote Terminal 1553 Status Word and Data Word(s) into the message block in the sequence in which they are to be transmitted over the 1553 bus. (See **3.4.1 Message Block Formats** on page 3-9.)

Note:

- The rules for the 1553 RT Status Word **do not** apply when simulating an RT: the user must provide the message Status Word; insert the 1760 header in the data; error injections and interrupts related to RTs are *not* available. (See **2.11.44 1553 RT Status Word Table** on page 2-38.)
- The **Service Request bit (SRQ)** is not supported in RT simulation.
- On a single function module (*PxS*) you cannot have a Concurrent RT when the module is in BC mode.

To indicate to the module which Remote Terminals are to be simulated, write to the 32-byte Active Remote Terminal table. Each entry in the 32-byte table corresponds to a specific Remote Terminal.

The first byte is for RT #0, the second is for RT #1, and the last byte is for RT #31 (for a total of 32 locations). A table entry value of 1 enables the Remote Terminal simulation by the module; a value of 0 disables the simulation by the module.

RT#31 RT Settings byte	341F H
RT#30 RT Settings byte	
• • •	• • •
RT#0 RT Settings byte	3400 H

Figure 3-8 RT Settings Table – BC/Concurrent RT mode

Bit	Description
01 – 07	Reserved – set to 0
00	1 = RT Active 0 = RT Not Active

RT Settings Byte Definition – BC/Concurrent RT mode

3.8 Continuous or One-Shot Message Transfers

The module can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

One-shot mode In One-Shot mode, after receiving a Start command, the module transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), turns off Bit 00 of the Start register, and waits for a new Start command. Use the Start Register to select One-Shot mode. See **3.13.9 Start Register** on page 3-22.

n-Times mode In n-Times mode, load the Loop Count register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start register. The user can transmit messages from 1 to 255 times. (See **3.13.9 Start Register** on page 3-22 and **3.13.13 Loop Count Register** on page 3-24.) The Frame Time registers, on page 3-29, determine the time between frames. See also **3.8.1 Frame Time Calculations** on page 3-15.

Continuous Loop mode In Continuous Loop mode, the module will retransmit the message frame at a predetermined, user-programmable rate. Use the Start register and the Loop Count register, to select Continuous Loop mode. (See **3.13.9 Start Register** on page 3-22 and **3.13.13 Loop Count Register** on page 3-24.) In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the module's operation by clearing Bit 00 of the Start register. See also **3.8.1 Frame Time Calculations** on page 3-15.

3.8.1 Frame Time Calculations

The Frame Time is a function of two control registers, the Frame Time Multiplier register and the Frame Time Resolution register. The internal Frame Time is loaded when a Start command is received. After all instructions are executed (1 frame), the module waits until the internal Frame Time counts down to 0 before reloading the Frame Time and transmits the next frame.

Note: If the Frame Time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 µsec, measured as dead time on the bus.

The module reads the **Frame Time Resolution Register**, multiplies it by the **Frame Time Multiplier Register**, and uses the product as the maximum number of 'clock ticks' to wait per frame. Each clock tick is 155 nanoseconds.

The maximum value of the Frame Time Resolution register is FFFF H (65535) 'clock ticks', which is equivalent to a frame time of:

FFFF (65535) × 155 nanoseconds per clock tick = 10158 microseconds

To enter a frame time up to 10158 microseconds, the Frame Time Multiplier register is 0 and

$$\text{desired resolution register} = \frac{\text{(desired time in microseconds)*1000}}{155}$$

To enter a Frame Time that is greater than 10158 microseconds, use the multiplier as well. For the greatest accuracy, the Frame Time Multiplier should have the minimum possible value.

The following algorithm first calculates the minimum Frame Time Multiplier and finds the appropriate resolution to obtain the desired frame time.

$$\text{frametime\_multiplier} = \frac{\text{desired time in microseconds}}{\text{10158 microseconds}}$$

$$\text{frametime\_resolution} = \left(\frac{\text{desired time in microseconds}}{\text{frametime\_ multiplier + 1}} \text{ X } 1000\right) / 155$$

Example: To calculate a Frame Time of 500 msec.

500 milliseconds = 500000 microseconds

$$\text{frametime\_multiplier} = \frac{500000}{10158} = 49$$

$$\text{frametime\_resolution} = \left(\left(\frac{500000}{49 + 1} \text{ X } 1000\right) / 155\right) = 64516$$

Frame Time Resolution = 64516 Dec (FC04 H)

Frame Time Multiplier = 50 Dec (0031 H)

Before issuing the Start command, set:

- The Frame Time Multiplier register to 0031 H
- The Frame Time Resolution register to FC04 H

For descriptions of these registers see **3.13.19 Frame Time Multiplier Register** on page 3-28 and **3.13.20 Frame Time Resolution Register** on page 3-28.

Note: The maximum frame time that the module can handle is 2.1 seconds (2,100,000 microseconds). To set this frame time, set the Frame Time Resolution register to FFA5 and Frame Time Multiplier register to 00CE. The minimum frame time is 0 microseconds.

3.9 Mode Codes

The module handles all dual-redundant 1553B Mode Codes; the Word Count field is decoded according to MIL-STD-1553B. The module does not implement the two Quad-redundant Mode Codes, Selected transmitter Shutdown and Override Selected transmitter Shutdown.

3.10 Service Request (SRQ) Processing

The SRQ bit is set by an RT in the 1553 RT Status Word (see **2.11.44 1553 RT Status Word Table** on page 2-38). Setting the SRQ bit indicates to the BC that the RT/ Subaddress requires servicing.

The BC provides the following service:

1. The module will send out a Mode Code 16 (transmit Vector Word) to get the Vector Word from the RT which contains more information about what needs service. This message is stored in SRQ Message 1 (3F80 – 3F87 H). See **3.13.31 SRQ Message 1 Register** on page 3-31.

2. The BC will then build and send out a transmit message (RT-to-BC) to this RT, with the Subaddress and Word Count as indicated in the corresponding bit positions of the Vector Word. This message is stored in SRQ Message 2 (3F88 – 3FCD H). See **3.13.30 SRQ Message 2 Register** on page 3-31 and **2.11.36 1553 RT Vector Word Table** on page 2-34.
3. If the interrupt SRQ message bit is set in the Interrupt Condition register (see **3.13.10 Interrupt Condition Register**, on page 3-22) an interrupt will be generated when the BC completes steps 1 and 2.
4. The SRQ Counter is incremented by 1. See **3.13.28 SRQ Counter** on page 3-30.

To disable Service Request processing set Bit 01 in the **3.13.40 BC Protocol Options Register** on page 3-34.

3.11 1760 Option

3.11.1 Header Word

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific Subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default module setting, or another value the user enters in the 1760 Header Value Transmit/ Receive Table.

1760 Header is not supported for RT-to-RT messages.

See **3.13.32 1760 Header Value Transmit Table**, **3.13.33 1760 Header Value Receive Table** and **3.13.34 1760 Header Exist Table** on page 3-32.

3.11.2 Checksum

The 1760 option implements checksum generation and checksum error detection capabilities. Checksums are calculated as each Data Word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last Data Word. On an incoming message, the calculated checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

The user gets to select, per message to generate or receive Checksum in the Intermessage Gap Time Counter. See **3.3.3 Intermessage Gap Time Counter/Message Function Select** on page 3-7.

If Checksum is selected the user may also request that the Checksum be sent out with an incorrect value as an error injection mechanism. See **3.3.3 Intermessage Gap Time Counter/Message Function Select** on page 3-7.

Note: For an RT-to-BC message where the RT is active, Checksums and headers are sent by specifying the header or the checksum in the message data. In this way header or checksum errors can be injected directly by the user.

3.12 Program Example: BC/Concurrent-RT Modes

The following two programming examples use the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

All values are in Hex unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,04`	Set the Configuration register to BC/RT mode.
`20 POKE &H3FF0,00`	Set the Message Stack Pointer registers to 0000.
`30 POKE &H3FF1,00`	(stack now begins at address: 0000)
`40 POKE &H3FF2,&HFF`	Set the Variable Amplitude register.
`50 POKE &H00,00`	Pointer to first message:
`60 POKE &H01,01`	(Location of message is 0100 H)
`70 POKE &H02,xx`	Set the Intermessage Gap Time location.
`80 POKE &H03,xx`	
`90 POKE &H08,&H40`	Pointer to second message:
`100 POKE &H09,01`	(Location of message is 0140 H)
`110 POKE &H0A,xx`	Set the Intermessage Gap Time location.
`120 POKE &H0B,xx`	
`130 POKE &H100,&H80`	Set the Control word to Transmit command,
`140 POKE &H101,00`	Bus A, and no errors injected.
`150 POKE &H102,&H23`	Set the Command Word to 0C23.
`160 POKE &H103,&H0C`	
`170 POKE &H104,&H00`	Set the Status Word to 0800.
`180 POKE &H105,&H08`	
`190 POKE &H106,&Hxx`	Set the Data Word to xxxx.
`200 POKE &H107,&Hxx`	
`210 POKE &H108,&Hyy`	Set the Data Word to yyyy.
`220 POKE &H109,&Hyy`	
`230 POKE &H10a,&Hzz`	Set the Data Word to zzzz.
`240 POKE &H10b,&Hzz`	
`250 POKE &H140,02`	Set the Control word to RT-to-RT command,
`260 POKE &H141,00`	Bus B, and no errors injected.
`270 POKE &H142,&H23`	Set the first (Receive) Command Word to 3823H.
`280 POKE &H143,&H38`	
`290 POKE &H144,&H43`	Set the second (Transmit) Command Word to 1C43H.
`300 POKE &H145,&H1C`	
`310 POKE &H3FEB,2`	Set the Instruction Counter to 2 (i.e., 2 messages)
`320 POKE &H3FEC,xx`	Set the Frame Time Resolution register.
`330 POKE &H3FED,xx`	
`340 POKE &H3FEE,xx`	Set the Frame Time Multiplier register
`350 POKE &H3FEF,XX`	
`360 POKE &H3401,1`	Enable RT #1. Use the Active RT’s Look-up Table to enable RTs. Module will simulate enabled RTs.
`370 POKE &H3FFC,1`	Set the Start register to 1. Starts message transfers in One-Shot mode.
`380 STOP`	

Program Example: BC/Concurrent for PCI[e] Carrier Boards – RT mode

BASIC Instruction	Remarks
`10 POKE &H3FFE,04`	Set the Configuration register to BC/RT mode.
`20 POKE &H3FF1,00`	Set the Message Stack Pointer registers to 0000.
`30 POKE &H3FF0,00`	(stack now begins at address: 0000)
`50 POKE &H01,00`	Pointer to first message:
`60 POKE &H00,01`	(Location of message is 0100 H)
`70 POKE &H03,xx`	Set the Intermessage Gap Time location.
`80 POKE &H02,xx`	
`90 POKE &H09,&H40`	Pointer to second message:
`100 POKE &H08,01`	(Location of message is 0140 H)
`110 POKE &H0B,xx`	Set the Intermessage Gap Time location.
`120 POKE &H0A,xx`	
`130 POKE &H101,&H80`	Set the Control word to Transmit command,
`140 POKE &H100,00`	Bus A, and no errors injected.
`150 POKE &H103,&H23`	Set the Command Word to 0C23.
`160 POKE &H102,&H0C`	
`170 POKE &H105,&H00`	Set the Status Word to 0800.
`180 POKE &H104,&H08`	
`190 POKE &H107,&Hxx`	Set the Data Word to xxxx.
`200 POKE &H106,&Hxx`	
`210 POKE &H109,&Hyy`	Set the Data Word to yyyy.
`220 POKE &H108,&Hyy`	
`230 POKE &H10B,&Hzz`	Set the Data Word to zzzz.
`240 POKE &H10A,&Hzz`	
`250 POKE &H141,02`	Set the Control word to RT-to-RT command,
`260 POKE &H140,00`	Bus B, and no errors injected.
`270 POKE &H143,&H23`	Set the first (Receive) Command Word to 3823H.
`280 POKE &H142,&H38`	
`290 POKE &H145,&H43`	Set the second (Transmit) Command Word to 1C43H.
`300 POKE &H144,&H1C`	
`310 POKE &H3FEA,2`	Set the Instruction Counter to 2 (i.e., 2 messages)
`320 POKE &H3FED,xx`	Set the Frame Time Resolution register.
`330 POKE &H3FEC,xx`	
`340 POKE &H3FEF,xx`	Set the Frame Time Multiplier register
`350 POKE &H3FEE,XX`	
`360 POKE &H3400,1`	Enable RT #1. Use the Active RT's Look-up Table to enable RTs. Module will simulate enabled RTs.
`370 POKE &H3FFD,1`	Set the Start register to 1. Starts message transfers in One-Shot mode.
`380 STOP`	

Program Example: BC/Concurrent for VME/VXI Carrier Boards – RT mode

3.13 Control Register Definitions

3.13.1 Instruction Stack/ Message Block Area — Address: 7100 – 7FFF (H)

This area is available to the programmer for Instruction Stacks and Message Blocks.

3.13.2 Time Tag — Address: 7008 – 700B (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon a power up or a software reset and starts counting. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

The counter must be read in the following sequence:

1. Read 7008 H – Lo word (16 bit, read only)
2. Read 700A H – Hi word (16 bit, read only)

The Time Tag resolution is 4 μsec.

To calculate elapsed time between Time Tags:

Example:

1. Calculate difference between Time Tags:
   150 (Time Tag 2) – 50 (Time Tag 1) = 100
2. Elapsed time:
   100 × 4 = 400 μsec

3.13.3 Time Tag Reset Register — Address: 7007 (H)

Write only

Write to the Time Tag Reset register to reset the module's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

3.13.4 Loopback Relay Select Register — Address: 7003 (H)

Write only

Write to the Loopback Relay Select register to activate an Onboard Loopback connection. The Onboard Loopback uses a series of onboard relays to enable you to perform an External Loopback Test without the use of an external cable. For information on running an External Loopback Test, see **Appendix D External Loopback Test** on page D-1.

Note: Onboard Loopback is only available with the -LB ordering option.

Bit	Bit Name	Description
03 – 07	Reserved	Set to 0
02	Loopback Relay	1 = Loopback relay active 0 = Normal operation
00 – 01	Reserved	Set to 0

Loopback Relay Select Register

Note: The Loopback Relay Select register is reset at power-up (all bits set to 0) or by a module reset.

3.13.5 Module Reset Register **Address: 7000 (H)**

Write any value to the Module Reset register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, module ID and Firmware Revision registers are written by the module after the reset operation is completed.

3.13.6 Module Configuration Register **Address: 3FFF (H)**

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration register.

To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

Hex Value	Operating Mode
04	BC/Concurrent-RT

Module Configuration Register Value: BC/RT Mode

3.13.7 Module ID Register **Address: 3FFE (H)**

The Module ID register contains a fixed value that can be read by your initialization function to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

3.13.8 Module Status Register **Address: 3FFD (H)**

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Always set
05 – 06	Indeterminate
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit is cleared in the Start register. Following this, the module sets Bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

3.13.9 Start Register Address: 3FFC (H)

The Start register controls the Start/Stop operation of the module. Writing the appropriate bit (Bit 00) to the Start register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, the user must set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the module resets the Start bit in the register after *all* messages have been transferred. The module does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set Bit 00 to 0. In order to halt the operation at the end of the entire frame, set Bit 02 to 0 (Bit 02 is not tested between message transfers). Related data Bit 04 in the Module Status register indicates when the module has been halted. (See **3.13.8 Module Status Register** on page 3-21.)

Bit	Description
03 – 07	0
02	1 = Loop mode 0 = One-Shot mode
01	0
00	1 = Start Operation 0 = Stop

Start Register

3.13.10 Interrupt Condition Register Address: 3FFB (H)

The Interrupt Condition register allows the user to set interrupt triggers. When a condition occurs that is enabled in this register, an interrupt is generated. A logic 1 enables the interrupt condition. To determine which condition caused the interrupt, check the Message Status register.

The Interrupt Condition register must be set before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

Bit	Description
06 – 07	0
05	SRQ message
04	End Minor Frame
03	Message Error
02	End of Frame
01	Message Complete
00	0

Interrupt Condition Register

Note: The interrupt will be sent at the end of the message for all interrupt conditions. When an interrupt is configured for an End of Frame or End

Minor Frame, the interrupt pulse occurs immediately after the last message transmission in the frame/minor frame is complete.

3.13.11 Message Status Register **Address: 3FFA (H)**

The Message Status register indicates the status of the current message being processed. The definition of each status bit is given below. Logic 1 indicates that the condition is activated.

Bit	Bit Name	Description
05 – 07	Reserved	Set to 0
04	End Minor Frame	The last word in the last message in the Minor Frame has been sent.
03	Message Error	The message has been sent. As a result, the Error bit has been set in the Message Status Word.
02	End Of Frame	The last word of the last message in the frame has been sent.
01	Message Complete	The last word of the message has been sent.
00	Wait For Continue	A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

Note: Status bits are *not* reset by the module. After reading them, the user must reset them.

3.13.12 RT Response Time Register **Address: 3FF9 (H)**

The RT Response Time register sets the Response Time of the Remote Terminals being simulated by the module. The resolution of the Response Time register is 155 nsec. per bit. The minimum time is approximately 4 μsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 μsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 μsec.

The Response Time register must be set before issuing a Start command to the module. To modify the RT Response Time register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22).

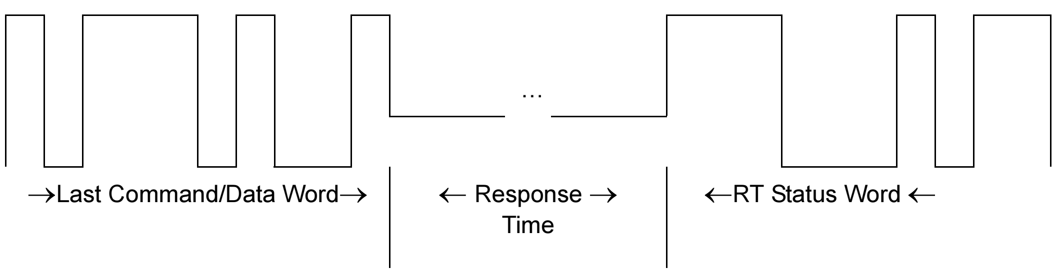


Figure 3-9 RT Response Time Definition

Example: To request a Response time of 9 µsec:
Write 32 to the RT Response Time register
$32 \times 0.155 \cong 5$ µsec + 4 µsec = 9 µsec

3.13.13 Loop Count Register

Address: 3FF6 (H)

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping.

The Loop Counter register must be set before issuing a Start command to the module. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

Bit	Value	Description
00 – 07	**0**	Transmits in Continuous Loop
	1 – 255	Sends Message Frame n-times as defined

Loop Count Register

3.13.14. Bit Error Register

Address: 3FF5 (H)

There are two types of bit errors, **Bit Count Error** and **Zero Crossing Error**. Both are enabled by setting the **Bit Error bit** (Bit 11), in the Control Word, see **3.4.2 Control Word** on page 3-11. The Bit Error register determines the nature of the error to be injected. If the Bit Error bit of the Control Word is not set, a valid 20-bit word is transmitted regardless of the contents of the Bit Error register.

Each of these errors can be injected into a Command Word or Data Word (see **Error Placement/Error Injection Enable bit**, (Bit 08), in the Control Word). If the error is to be injected in a Data Word, the Data Word is selected via the Error Word Index register, see **3.13.26 Error Word Index Register** on page 3-30.

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

3.13.14.1 Bit Count Error

The total number of bits sent in a 1553 Word, including Sync (3) and Parity (1) is more or less than the normal 20 bits.

The bit count is selected using bits 00 – 02 of the Bit Error register.

Bit	Description			
00 – 02	Bit 02	Bit 01	Bit 00	Number of 1553 bits sent per word
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Error Register Bit Count Error Settings

3.13.14.2 Zero Crossing Error

The bit pattern is altered, from normal Manchester II zero cross coding to a skewed form of the coding. Zero Crossing error will affect the bit selected via the Zero Cross Bit Index register. See **3.13.25 Zero Cross Bit Index Register** on page 3-30.

The Zero Cross coding is selected using bits 04 – 07 of the Bit Error register:

Bit	Description				
04 – 07	Bit 07	Bit 06	Bit 05	Bit 04	Zero crossing coding used
	0	0	0	0	zc at 500 nano (normal)
	0	0	0	1	zc at 600 nano (legal)
	0	0	1	0	zc at 650 nano (illegal)
	0	0	1	1	zc at 700 nano (illegal)
	0	1	0	0	zc at 400 nano (legal)
	0	1	0	1	zc at 350 nano (illegal)
	0	1	1	0	zc at 300 nano (illegal)
	0	1	1	1	Reserved
	1	0	0	0	full bit high
	1	0	0	1	full bit low
	1	0	1	0	full bit dead
	Other values				Reserved

Bit Error Register Zero Crossing Error Settings

Bit 03 of the Bit Error register is reserved.

Set the Bit Error register before issuing a Start command to the module. To modify the Bit Error register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

3.13.15 Word Count Register **Address: 3FF4 (H)**

The Word Count register controls the number of 1553 Data Words (±3) in the message and allows the user to inject a Word Count error. The error is an offset relative to the 1553 Command Word Word Count field. This register is used by the Module only for messages for which the Word Count Error bit is set in the Control word register. (See **3.4.2 Control Word** on page 3-11.) If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count register.

The Word Count register must be set before issuing a Start command to the module. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

Register Value	Word Count Offset
FD H	-3 Words
FE H	-2 Words
FF H	-1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Register Values

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

3.13.16 BC Response Time Register **Address: 3FF3 (H)**

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum wait time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, The minimum time is approximately 2 µsec.

The BC Response Time register must be set before issuing a Start command to the module. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

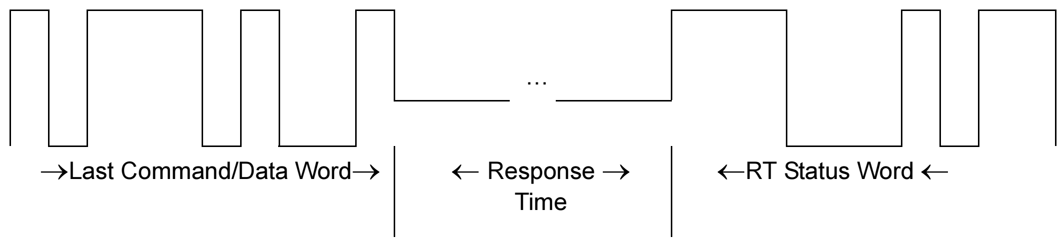


Figure 3-10 BC Response Time Definition

Example: To request a Response time of 14 μsec:
Write 90 to the BC Response Time register
$90 \times 0.155 \cong 14$ μsec

3.13.17 Variable Amplitude Register — Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.0 volts (peak-to-peak) when measured on the 1553 bus using Direct Coupling mode and 39-Ohm load (that is, two 78-Ohm termination resistors). The Variable Amplitude register has a resolution of 28 mV/bit (p-p) on the bus.

These values are correct on an ideal system. In practice, the actual signal amplitude can vary approximately ±1 volt (p-p) depending on the characteristics of the system components (cables, connectors, transformers, couplers, etc.). In addition, the more bus connections (bus load) the more the actual amplitude is reduced.

Set the Variable Amplitude register before issuing a Start command to the module. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.) After a reset, the Variable Amplitude register defaults to FF (H), providing maximum amplitude.

Note: On a single function module (*PxS*), the amplitude is not variable and is set to 7.0 volts (p-p).

3.13.18 Message Stack Pointer — Address: 3FF0 – 3FF1 (H)

The Message Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 – 33FF (H), 4000 – 6FFF (H) and 7100 – 7FFF (H).

The Stack Pointer register must be set before issuing a Start command to module. To modify the Stack Pointer register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

3.13.19 Frame Time Multiplier Register Address: 3FEE – 3FEF (H)

The Frame Time Multiplier register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time Multiplier register is multiplied by the value set in the Frame Time Resolution register described below. The value set must equal the desired multiplication factor -1.

The Frame Time Multiplier register must be set before issuing a Start command to the module. To modify the Frame Time Multiplier register, issue a Stop command, modify the register, then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

For information on how to use Frame Times, see **3.8.1 Frame Time Calculations** on page 3-15.

3.13.20 Frame Time Resolution Register Address: 3FEC – 3FED (H)

The 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. (See **3.8 Continuous or One-Shot Message Transfers** on page 3-15.)

The Frame Time Resolution register must be set before issuing a Start command to the module. For an example of how to calculate Frame Time Multiplier and Frame Time Resolution, see **3.8 Continuous or One-Shot Message Transfers** on page 3-15. To modify the Frame Time Resolution register, issue a Stop command, modify the register, then, issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

For information on how to use Frame Times, see **3.8.1 Frame Time Calculations** on page 3-15.

3.13.21 Instruction Counter Address: 3FEB, 3FEA (H)

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before the user writes to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The module updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

The Instruction Counter register must be set before issuing a Start command to the module. To modify the Instruction Counter register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.) When in Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

The low register (3FEA H) contains the MSB; the high register (3FEB H) contains the LSB. Therefore, for an Instruction Counter less than 256, use the LSB only, address 3FEB H.

3.13.22 Minor Frame Time Register — Address: 3FE8 – 3FE9 (H)

Write only

This 16-bit Minor Frame Time register is used to set the length of a single minor frame. (See **3.5 Minor Frame Operation** on page 3-13.) The resolution of the Minor Frame Time register is 1 μsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Multiplier register.

The Minor Frame Time register must be set before issuing a Start command to the module. To modify the Minor Frame Time register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

3.13.23 Minor Frame Time Multiplier Register — Address: 3FE6 – 3FE7 (H)

Write only

The Minor Frame Time Multiplier register is a multiplier of the Minor Frame Time register described above. The value written by the user to the Minor Frame Time Multiplier register allows the user to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time register. The maximum Minor Frame Time Multiplier is 255. The maximum Minor Frame Time possible using both registers is approximately 800 milliseconds.

Example: To generate a Minor Frame Time of 1 sec., set the Minor Frame Time register to F424 H (62,500 Dec.), and set the Minor Frame Time Multiplier register to 10 H (16 Dec.).

The Minor Frame Time Multiplier register must be set before issuing a Start command to the module. To modify the Minor Frame Time Multiplier register, issue a Stop command, modify the register, and then issue a Start command. (See **3.13.9 Start Register** on page 3-22.)

3.13.24 Replay Register — Address: 3FE4 – 3FE5 (H)

Regular message processing is accomplished using Intermessage Time Gaps between messages. The module waits between messages as per the intermessage gap time.

With the Replay register, the user sets the *absolute time* at which each message is to be transmitted over the bus. The Bus Controller compares this absolute time with its internal Time Tag to determine if the time has come to transmit the message over the bus. Generally the user will reset the BC's Time Tag just prior to running and will select time absolute time 0 for the first message to be transmitted.

For example, the user may request that the first message be transmitted at time 1000 microseconds, the second message at 2000 microseconds and so on.

This timing method is useful for replaying a previously recorded scenario based on the recorded Time Tags.

The absolute time is set by the user in units of 32 microseconds.

Bit	Description
01 – 15	Reserved
00	1 = Replay mode 0 = Intermessage gap mode

Replay register

3.13.25 Zero Cross Bit Index Register — Address: 3FDC – 3FDD (H)

When a zero cross error is injected into a Message (see **3.13.14 Bit Error Register** on page 3-24), this register determines which bit within the word will contain the error. A zero in this register will cause the error to be injected into the first Data Word, a 1 into the second bit etc. Valid values for this register are 0 through 15.

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

3.13.26 Error Word Index Register — Address: 3FDA – 3FDB (H)

When a data error is injected into a Message (see **3.4.2 Control Word** on page 3-11), this register determines which error word will contain the error. A zero in this register will cause the error to be injected into the first Data Word, a 1 into the second word etc. If the number is greater than the number of words in the message, no error will be injected.

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

3.13.27 Sync Pattern Register — Address: 3FD8 – 3FD9 (H)

The low six bits of this register each represent a half bit time for use in sync error error injection. (See Bit 10 of the Control Word, **3.4.2 Control Word** on page 3-11.) When the sync error is requested and the BC Protocol register Bit 02 is set, the sync will be transmitted according to the pattern set in this register. A 0023 H in this register (100011 binary) would be sent as one bit times high, three bit times low and two bit times high.

See **3.13.40 BC Protocol Options Register** on page 3-34.

Note: On a single function module (*PxS*) this register is reserved. Error injection is not available.

3.13.28 SRQ Counter — Address: 3FD2 – 3FD3 (H)

The SRQ counter contains the number of messages processed since BC was run.

See **3.10 Service Request (SRQ) Processing** on page 3-16.

3.13.29 SRQ Message Status Register — Address: 3FCE – 3FD1 (H)

The SRQ Message Status Register contains the SRQ Message 1 at 3FCE (H) and SRQ Message 2 at 3FD1H).

See **3.10 Service Request (SRQ) Processing** on page 3-16.

3.13.30 SRQ Message 2 Register — Address: 3F88 – 3FCD (H)

The SRQ Message 2 register contains the Transmit message sent to the Subaddress identified in the Vector word received from SRQ processing. The message consists of:

Control Word	Command Word	1553 Status Word	Up to 32 Data Words

See **3.10 Service Request (SRQ) Processing** on page 3-16.

3.13.31 SRQ Message 1 Register — Address: 3F80 – 3F87 (H)

The SRQ Message 1 register contains the Transmit Vector Mode Code message sent out by the BC in response to SRQ by an RT. The message consists of:

Control Word	Command Word	1553 Status Word	Vector Word

See **3.10 Service Request (SRQ) Processing** on page 3-16.

3.13.32 1760 Header Value Transmit Table — Address: 3F40 – 3F7F (H)

1760 Option only

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message. The module checks that the specified Header receive value was received. In addition, the Internal Concurrent monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header Error** bit is set in the Message Status Word. See **3.3.1 Message Status Word** on page 3-6.

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

Transmit Subaddress	Header Value	Address
1	**0421 H**	3F42 H
11	**0420 H**	3F56 H
14	**0423 H**	3F5C H

Predefined 1760 Transmit Header Values

3.13.33 1760 Header Value Receive Table

Address: 3F00 – 3F3F H

1760 Option only

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. If the wrong data was sent, the Internal Concurrent Monitor will set an error bit. See Bit 06 of the Message Status Word (**3.3.1 Message Status Word** on page 3-6).

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

Receive Subaddress	Header Value	Address
11	**0400 H**	3F16 H
14	**0422 H**	3F1C H

Predefined 1760 Receive Header Values

3.13.34 1760 Header Exist Table

Address: 3EC0 – 3EFF (H)

1760 Option only

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for RT-to-BC or RT-to-RT messages directed to that Subaddress.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on each module.

To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value (Transmit/Receive) Table.

Bit	Description
09-15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC or RT-to-RT) 0 = Module should **not** expect a Header word in a transmit message
01 – 07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should **not** expect a Header word in a receive message

1760 Header Exist Table

Subaddress	Header Value	Address
1	**0100 H**	3EC2 H
11	**0101 H**	3ED6 H
14	**0101 H**	3EDC H

Predefined 1760 Headers

3.13.35 Module Time Register Lo & Hi

Address: 3EA4 – 3EA5 (H)
3EA2 – 3EA3 (H)

This register holds the module time value, which is stored in non-volatile flash memory and loaded at power-up. This value can be modified by calling the Set_ModuleTime_Px function. (See the *1553Px Family Software Tools Programmer's Reference*.) The factory default value is FFFF FFFF (H).

3.13.36 Serial Number Register

Address: 3EA0 – 3EA1 (H)

This register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660 (decimal).

3.13.37 Error Counter Lo & Hi

Address: 3E9E – 3E9F (H)
3E9C – 3E9D (H)

Error Counter is a running 32-bit counter of message errors. The counter counts retries separately.

3.13.38 Message Counter Lo & Hi

Address: 3E9A – 3E9B (H)
3E98 – 3E99 (H)

Message Counter is a running 32-bit counter of all messages received. The counter counts retries separately.

3.13.39 Module Function Register

Address: 3E8E – 3E8F (H)

Set Bit 00 of the Module Function register to 1 to expand the Message Block Area. When the Message Block Area is expanded, there is no Concurrent Monitor. Note that in most cases it is not recommended to use Expanded Block mode in BC/Concurrent-RT mode, since the standard Message Block Area is generally sufficient.

3.13.40 BC Protocol Options Register **Address: 3E8C – 3E8D (H)**

Bit	Description
04	1 = Adds intermessage gap time when skipping a message. See **3.4.4 Skip Message** on page 3-12. 0 = Does not add intermessage gap time when skipping a message
03	1 = 250 nsec intermessage gap time resolution 0 = 1 µsec intermessage gap time resolution (default)
02	1 = Enable Sync Pattern Error injection. If this bit is set, Sync Errors are injected based on the Sync Pattern register. (See **3.13.27 Sync Pattern Register** on page 3-30.) 0 = Disable Sync Pattern Error injection. Sync Errors in Command Words will cause Data Sync to be sent and Sync Error in Data Words will cause Command Sync to be sent.
01	1 = Disable SRQ processing. If this bit is set, SRQ bit in the RT Status Word is ignored. See **3.10 Service Request (SRQ) Processing** on page 3-16. 0 = Enable SRQ processing
00	1 = Simulate MIL-STD-1553A protocol. If set to 1553A protocol, Mode Codes are assumed not to have any data. 0 = Simulate MIL-STD-1553A protocol

More Module Options Register

3.13.41 Send Time Tag on Sync Register **Address: 3E8A – 3E8B (H)**

Set the Send Time Tag on Sync register to indicate that the module should send the current Time Tag value (with a resolution of 64 µsec.) as the 16-bit Data Word upon transmitting a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

3.13.42 Clear Time Tag on Sync Register **Address: 3E88 – 3E89 (H)**

Write 1 to the lower byte (3E88 H) of the Clear Time Tag on Sync register to indicate that the module should clear the Time Tag counter (7008 – 700B H) (reset to 0) upon the transmission of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Write 1 to the higher byte (3E89 H) of the Clear Time Tag on Sync register to indicate that the module should clear the Time Tag counter (7008 – 700B H) (reset to 0) upon the transmission of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

Note: This register setting does not take effect until the module is restarted.

3.13.43 More Module Options Register — Address: 3E86 – 3E87 (H)

Read only The More Module Options register is a 16-bit register that provides additional module information.

Bit	Description
06 – 15	Reserved
05	1 = Expanded Block mode is available in BC mode 0 = Expanded Block mode is not available in BC mode
04	1 = Enhanced Monitor mode is available in Sequential Fixed-Block Monitor mode 0 = Enhanced Monitor mode is not available in Sequential Fixed-Block Monitor mode
03	1 = Expanded Block mode is available in Sequential Fixed-Block Monitor mode 0 = Expanded Block mode is not available in Sequential Fixed-Block Monitor mode
02	1 = Module is single function (*PxS*) 0 = Module is multifunction (*Px*)
01	1 = Onboard Loopback option is available 0 = Onboard Loopback option is not available
00	1 = Module is only available in Monitor mode 0 = Module is available in all modes

More Module Options Register

3.13.44 Module Options Register — Address: 3E84 – 3E85 (H)

Read only The Module Options register is a 16-bit register that provides information about the internal processor and firmware.

Bit	Description
15	1 = PxIII
14	Reserved – set to 1
13	1 = Expanded Block mode is in use in RT mode
12	1 = Module is on a removable card (PCMCIA or ExpressCard) 0 = Module is on an add-in board
11	1 = Replay mode is in use (BC mode only)
10	1 = PxII
09	1 = 1760
08	1 = 1553
00 – 07	4D H Always set; indicates Internal Concurrent Monitor

Module Options Register

3.13.45 Firmware Revision Register — Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-module firmware. The value 18 (H) would be read as revision level: 1.8.

3.13.46 Asynchronous Start Flag Register — Address: 3424 – 3425 (H)

Write only To indicate that it is now time to send a selected frame asynchronously, write a 1 to the Asynchronous Start Flag register. The module will automatically reset this value to 0 when it sends the frame.

3.13.47 Asynchronous Frame Pointer Register — Address: 3422 – 3423 (H)

Write only To send asynchronously to this register, write the address at the beginning of the selected frame.

3.13.48 Asynchronous Message Count Register — Address: 3420 – 3421 (H)

Write only Write the number of messages contained in the Asynchronous Frame. The maximum number of messages allowed in a frame is determined by the amount of available space in the message stack area of the module and the size of the individual messages.

4 Bus Monitor Operation

Chapter 4 describes module operation in Bus Monitor mode. The topics covered are:

4.1 Bus Monitor Mode Overview

The Bus Monitor can operate in one of two modes, Sequential mode and Look-up Table mode:

Sequential mode: 1553 Message Blocks are stored in sequential locations in memory. Sequential mode supports two types of operations, Fixed-Block and Linked-List:

Fixed-Block operation: 1553 messages are stored at fixed sequential blocks in the memory. Sequential Fixed-Block mode supports Trigger capability.

When using Fixed-Block operation, you have the following options, Regular Monitor, Expanded Monitor and Enhanced Monitor. For more information on these modes, see **4.4.1 Message Block Fixed-Block Operation** on page 4-7. To check whether your module supports Expanded Monitor or Enhanced Monitor, use the **4.13.32 More Module Options Register** on page 4-34.

Linked-List operation: 1553 messages are packed one after another in the memory, separated by a header.

Look-up Table mode: Each 1553 message is stored in a unique Message Block. In Look-up Table mode, the module addresses the user-programmable Look-up Table when it receives a 1553 Command Word. The Command Word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-up Table with 2048 (2K × 8) locations.

Use the Module Configuration Register to program the desired mode of operation. See **4.13.5 Module Configuration Register** on page 4-25.

To determine if the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID register (test for value = 45 H).
2. Check the Module Status register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a 1 to the Start register is referred to as issuing a Start command.

4.2 Sequential Fixed-Block Memory Map

The following memory maps show the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

Reserved	FCB0 – FFFF H
Fourth Message Block Area (400 Blocks)[1]	7FB0 – FCAF H
Third Message Block Area (47 Blocks)	7100 – 7FAF H
Reserved	700C – 70FF H
Time Tag (Hi)	700A – 700B H
Time Tag (Lo)	7008 – 7009 H
Time Tag Reset Register	7007 H
Reserved	7004 – 7006 H
Internal Monitor Connect Register	7003 H
Reserved	7001 – 7002 H
Module Reset Register	7000 H
Reserved	6FD1 – 6FFF H
Second Message Block Area (153 Blocks)	4000 – 6FD0 H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF8 – 3FF9 H
Time Tag Resolution Register	3FF7 H
Reserved	3FF6 H
Current Message Block Register	3FF5 H
Block Trigger Value Register	3FF4 H
Trigger Word #1	3FF2 – 3FF3 H
Trigger Mask #1	3FF0 – 3FF1 H
Trigger Word #2	3FEE – 3FEF H
Trigger Mask #2	3FEC – 3FED H
Trigger Control Register	3FEB H

Mode Code Control Register	3FEA H
Broadcast Control Register	3FE8 – 3FE9 H
Reserved	3F80 – 3FE7 H
1760 Header Value Transmit Table[2]	3F40 – 3F7F H
1760 Header Value Receive Table[2]	3F00 – 3F3F H
1760 Header Exist Table[2]	3EC0 – 3EFF H
Expanded Current Message Block Register	3EBE – 3EBF H
Reserved	3EAC – 3EBD H
Pretrigger Message Counter (Lo)	3EAA –3EAB H
Pretrigger Message Counter (Hi)	3EA8 –3EA9 H
Reserved	3EA6 – 3EA7 H
Module Time Register (Lo)	3EA4 – 3EA5 H
Module Time Register (Hi)	3EA2 – 3EA3 H
Serial Number Register	3EA0 – 3EA1 H
Error Counter (Lo)	3E9E – 3E9F H
Error Counter (Hi)	3E9C – 3E9D H
Message Counter (Lo)	3E9A – 3E9B H
Message Counter (Hi)	3E98 – 3E99 H
Reserved	3E90 – 3E97 H
Monitor Response Time Reg.	3E8E – 3E8F H
1553A Register	3E8C – 3F8D H
Module Function Register	3E8A – 3E8B H
Clear Time Tag on Sync Register	3E88 – 3E89 H
More Module Options Register	3E86 – 3E87 H
Module Options Register	3E84 – 3E85 H
Reserved	3E81 – 3E83 H
Firmware Revision Register	3E80 H
Message Block Area (200 Blocks)	0000 – 3E7F H

Figure 4-1 Bus Monitor – Sequential Fixed-Block Memory Map for PCI[e] Carrier Boards

1. These 400 blocks are either used for Expanded Monitor or for the additional information saved when using Enhanced Monitor.
2. 1760 Option only

Reserved	FCB0 – FFFF H	Broadcast Control Register	3FE8 – 3FE9 H
Fourth Message Block Area (400 Blocks)[1]	7FB0 – FCAF H	Reserved	3F80 – 3FE7 H
Third Message Block Area (47 Blocks)	7100 – 7FAF H	1760 Header Value Transmit Table[2]	3F40 – 3F7F H
Reserved	700C – 70FF H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Time Tag (Hi)	700A – 700B H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Time Tag (Lo)	7008 – 7009 H	Expanded Current Message Block Register	3EBE – 3EBF H
Reserved	7007 H	Reserved	3EAC – 3EBD H
Time Tag Reset Register	7006 H	Pretrigger Message Counter (Lo)	3EAA –3EAB H
Reserved	7003 – 7005 H	Pretrigger Message Counter (Hi)	3EA8 – 3EA9 H
Internal Monitor Connect Register	7002 H	Reserved	3EA6 – 3EA7 H
Module Reset Register	7001 H	Module Time Register (Lo)	3EA4 – 3EA5 H
Reserved	6FD1 – 6FFF H	Module Time Register (Hi)	3EA2 – 3EA3 H
Second Message Block Area (153 Blocks)	4000 – 6FD0 H	Serial Number Register	3EA0 – 3EA1 H
Module ID Register	3FFF H	Error Counter (Lo)	3E9E – 3E9F H
Module Configuration Register	3FFE H	Error Counter (Hi)	3E9C – 3E9D H
Start Register	3FFD H	Message Counter (Lo)	3E9A – 3E9B H
Module Status Register	3FFC H	Message Counter (Hi)	3E98 – 3E99 H
Message Status Register	3FFB H	Reserved	3E90 – 3E97 H
Interrupt Condition Register	3FFA H	Monitor Response Time Reg.	3E8E – 3E8F H
Reserved	3FF7 – 3FF9 H	1553A register	3E8C – 3F8D H
Time Tag Resolution Register	3FF6 H	Module Function Register	3E8A – 3E8B H
Block Trigger Value Register	3FF5 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
Current Message Block Register	3FF4 H	More Module Options Register	3E86 – 3E87 H
Trigger Word #1	3FF2 – 3FF3 H	Module Options Register	3E84 – 3E85 H
Trigger Mask #1	3FF0 – 3FF1 H	Reserved	3E82 – 3E83 H
Trigger Word #2	3FEE – 3FEF H	Firmware Revision Register	3E81 H
Trigger Mask #2	3FEC – 3FED H	Reserved	3E80 H
Mode Code Control Register	3FEB H	Message Block Area (200 Blocks)	0000 – 3E7F H
Trigger Control Register	3FEA H		

Figure 4-2 Bus Monitor: Sequential Fixed-Block Memory Map for VME/VXI Carrier Boards

1. These 400 blocks are either used for Expanded Monitor or for the additional information saved when using Enhanced Monitor.
2. 1760 Option only

4.3 Sequential Linked-List Memory Map

The following memory maps show the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

Reserved	700C – FFFF H	Broadcast Control Register	3FE8 – 3FE9 H
Time Tag (Hi)	700A – 700B H	1760 Header Value Transmit Table[1]	3F40 – 3F7F H
Time Tag (Lo)	7008 – 7009 H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Time Tag Reset Register	7007 H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Reserved	7004 – 7006 H	Reserved	3FA6 – 3FBF H
Internal Monitor Connect Register	7003 H	Module Time Register (Lo)	3EA4 – 3EA5 H
Reserved	7001 – 7002 H	Module Time Register (Hi)	3EA2 – 3EA3 H
Module Reset Register	7000 H	Serial Number Register	3EA0 – 3EA1 H
Reserved	4000 – 6FFF H	Error Counter (Lo)	3E9E – 3E9F H
Module Configuration Register	3FFF H	Error Counter (Hi)	3E9C – 3E9D H
Module ID Register	3FFE H	Message Counter (Lo)	3E9A – 3E9B H
Module Status Register	3FFD H	Message Counter (Hi)	3E98 – 3E99 H
Start Register	3FFC H	Reserved	3E90 – 3E97 H
Interrupt Condition Register	3FFB H	Monitor Response Time Reg.	3E8E – 3E8F H
Message Status Register	3FFA H	1553A Register	3E8C – 3E8D H
Reserved	3FF8 – 3FF9 H	Initial Link Register	3E8A – 3E8B H
Time Tag Resolution Register	3FF7 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
Reserved	3FF6 H	More Module Options Register	3E86 – 3E87 H
End Buffer Pointer	3FF4 – 3FF5 H	Module Options Register	3E84 – 3E85 H
Next Message Pointer	3FF2 – 3FF3 H	Reserved	3E81 – 3E83 H
Reserved	3FEB – 3FF1 H	Firmware Revision Register	3E80 H
Mode Code Control Register	3FEA H	Message Block Spill Area	3E00 – 3E7F H
Broadcast Control Register	3FE8 – 3FE9 H	Message Block Area	0000 – 3DFF H

Figure 4-3 Bus Monitor – Sequential Linked-List Memory Map for PCI[e] Carrier Boards

1. 1760 Option only

Reserved	700C – FFFF H		
Time Tag (Hi)	700A – 700B H	1760 Header Value Transmit Table[1]	3F40 – 3F7F H
Time Tag (Lo)	7008 – 7009 H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Reserved	7007 H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Time Tag Reset Register	7006 H	Reserved	3EA6 – 3EBF H
Reserved	7003 – 7005 H	Module Time Register (Lo)	3EA4 – 3EA5 H
Internal Monitor Connect Register	7002 H	Module Time Register (Hi)	3EA2 – 3EA3 H
Module Reset Register	7001 H	Serial Number Register	3EA0 – 3EA1 H
Reserved	4000 – 7000 H	Error Counter (Lo)	3E9E – 3E9F H
Module ID Register	3FFF H	Error Counter (Hi)	3E9C – 3E9D H
Module Configuration Register	3FFE H	Message Counter (Lo)	3E9A – 3E9B H
Start Register	3FFD H	Message Counter (Hi)	3E98 – 3E99 H
Module Status Register	3FFC H	Reserved	3E90 – 3E97 H
Message Status Register	3FFB H	Monitor Response Time Reg.	3E8E – 3E8F H
Interrupt Condition Register	3FFA H	1553A Register	3E8C – 3E8D H
Reserved	3FF7 – 3FF9 H	Initial Link Register	3E8A – 3E8B H
Time Tag Resolution Register	3FF6 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
End Buffer Pointer	3FF4 – 3FF5 H	More Module Options Register	3E86 – 3E87 H
Next Message Pointer	3FF2 – 3FF3 H	Module Options Register	3E84 – 3E85 H
Reserved	3FEC – 3FF1 H	Reserved	3E82 – 3E83 H
Mode Code Control Register	3FEB H	Firmware Revision Register	3E81 H
Reserved	3FEA H	Reserved	3E80 H
Broadcast Control Register	3FE8 – 3FE9 H	Message Block Spill Area	3E00 – 3E7F H
Reserved	3F80 – 3FE7 H	Message Block Area	0000 – 3DFF H

Figure 4-4 Bus Monitor: Sequential Linked-List Memory Map for VME/VXI Carrier Boards

1. 1760 Option only

4.4 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned into either blocks of fixed length or into a Linked-List of blocks of varying lengths. The Module Configuration Register determines the type of partitioning. See **4.13.5 Module Configuration Register** on page 4-25.

For a description of the Time Tag function, see **4.8 Time Tag Word** on page 4-16.

4.4.1 Message Block Fixed-Block Operation

When using Fixed-Block operation, you have the following options:

- **Regular Monitor:** 200 blocks are used to store Bus Monitor data.
- **Expanded Monitor:** 800 blocks are used to store Bus Monitor data.
- **Enhanced Monitor:** 400 blocks are used to store Bus Monitor data, and an additional 400 blocks are used to store additional information about each word.

  For more information, see**4.4.1.1 Expanded Monitor** on page 4-8.

In Fixed-Block operation, the Message Block area is divided into 200, 400 or 800 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation. (See **4.10 Trigger Operation** on page 4-17.)

Figure 4-5 shows the memory map of each block.

Information is stored in the memory in the following sequence	Byte offset
Message Counter (Lo)	+78
1553 Data Word	•
•	•
•	•
•	•
1553 Data Word	+8
1553 Command Word	+6
Time Tag (Hi)	+4
Time Tag (Lo)	+2
Message Status Word	0

Figure 4-5 Bus Monitor Message Block – Fixed-Block Operation

4.4.1.1 Expanded Monitor

Expanded Monitor uses 800 blocks to store Bus Monitor data (instead of 200 blocks when using Regular Monitor). When using Expanded Monitor, each block is the same as shown in Figure 4-5. Use the **4.13.30 Module Function Register** on page 4-33, for setting Expanded Monitor.

Note: Expanded Monitor is only available in Sequential Monitor mode in Fixed-Block operation. To check whether your module supports Expanded Monitor mode, use the **4.13.32 More Module Options Register** on page 4-34.

4.4.1.2 Enhanced Monitor

Enhanced Monitor uses 400 blocks for Bus Monitor data, and an additional 400 blocks for additional information about each word. The blocks in the first 400 blocks correspond to the blocks in the additional 400 blocks. For example, block 1 in the regular message buffer corresponds to block 1 of the additional information buffer. The

When using Enhanced Monitor, all words are saved, including those with errors. For example, Data Words without Command Words are saved. When using Regular Monitor or Expanded Monitor, these are disregarded. When an error message has more than 36 words, the message is stored in two or more data blocks, the first 36 words in the first data block, and the remainder in the next data block(s). Use the **4.13.30 Module Function Register** on page 4-33, for setting Enhanced Monitor.

Note: Enhanced Monitor is only available in Sequential Monitor mode in Fixed-Block operation. To check whether your module supports Enhanced Monitor mode, use the **4.13.32 More Module Options Register** on page 4-34.

Figure 4-6 shows the memory map of each block of additional information when using Enhanced Monitor.

Information is stored in the memory in the following sequence	Byte offset
Message Counter (Lo)	+78
Additional Message Info	+76
•	•
•	•
•	•
Additional Message Info	+6
Reserved	+4
Reserved	+2
Enhanced Message Status Word	0

Figure 4-6 Bus Monitor Message Block: Additional Information Block in Enhanced Monitor

The bits of the Additional Message Info are as follows:

Bit	Description
12 – 15	‘C’ = Command (or Status) Word sync pattern ‘D’ = Data Word sync pattern
08 – 11	‘A’ = Word was received on Bus A ‘B’ = Word was received on Bus B
04 – 07	‘0’ = Word was received contiguously with the previous word ‘1’ = Word was received non-contiguously
03	Set to 0
02	Set to 0
01	0 = No Manchester error occurred 1 = Manchester error occurred
00	0 = No Parity error occurred 1 = Parity error occurred

Additional Information

The bits of the Enhanced Message Status Word are as follows:

Bit	Description
15	1 = End of message; message transfer completed.
06 – 14	Reserved
00 – 05	Number of words in the block

Enhanced Message Status Word

4.4.2 Message Block Linked-List Operation

In Linked-List operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each block comprise the message header. This header contains the address of the next Message Block header. The header of the last 1553 block received contains *xx*FF (End of File), indicating that there are no more messages stored. After a message is processed and stored in memory, the header of the preceding message block is updated from *xx*FF to the address (of the header in the block) of the newly stored message.

The Linked-List method can store more data than Fixed-Block operation.

The buffer never wraps around in the middle of a message. When the buffer is full, or if there is no room left to store the entire next message, the next message will be stored in the first location of the Message Block Area (0000 H). The header of the last message will point to that location in the Message Block Area. In this special case, to know exactly where the message ends, use the End Buffer Pointer. The End Buffer Pointer points to the address after the last location of the message, indicating the length of the message. See **4.13.14 End Buffer Pointer** on page 4-28.

Figure 4-7 illustrates the contents of the Message block. For a description of the Time Tag function, see **4.8 Time Tag Word** on page 4-16.

Information is stored in the memory in the following sequence:	Byte Offset
End Of File: XXFF	•
1553 Data Word	•
•	•
•	•
•	•
1553 Data Word	+A
1553 Command Word	+8
Time Tag (Hi)	+6
Time Tag (Lo)	+4
Message Status Word	+2
Message Header - Address of Next Block	0

Figure 4-7 Bus Monitor Message Block – Linked-List Operation

4.5 Look-up Table Mode Memory Map

The following memory maps show the addresses for PCI[e] carrier boards and for VME/VXI carrier boards. For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

Reserved	700C – FFFF H	Broadcast Control Register	3FE8 – 3FE9 H
Time Tag (Hi)	700A – 700B H	Reserved	3F80 – 3FE7 H
Time Tag (Lo)	7008 – 7009 H	1760 Header Value Transmit Table[1]	3F40 – 3F7F H
Time Tag Reset Register	7007 H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Reserved	7004 – 7006 H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Internal Monitor Connect Register	7003 H	Reserved	3FA6 – 3FBF H
Reserved	7001 – 7002 H	Module Time Register (Lo)	3EA4 – 3EA5 H
Module Reset Register	7000 H	Module Time Register (Hi)	3EA2 – 3EA3 H
Reserved	4800 – 6FFF H	Serial Number Register	3EA0 – 3EA1 H
Data Block Look-up Table (2K × 8)	4000 – 47FF H	Error Counter (Lo)	3E9E – 3E9F H
Module Configuration Register	3FFF H	Error Counter (Hi)	3E9C – 3E9D H
Module ID Register	3FFE H	Message Counter (Lo)	3E9A – 3E9B H
Module Status Register	3FFD H	Message Counter (Hi)	3E98 – 3E99 H
Start Register	3FFC H	Reserved	3E90 – 3E97 H
Interrupt Condition Register	3FFB H	Monitor Response Time Register	3E8E – 3E8F H
Message Status Register	3FFA H	1553A Register	3E8C – 3E8D H
Reserved	3FF8 – 3FF9 H	Reserved	3E8A – 3E8B H
Time Tag Resolution Register	3FF7 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
Reserved	3FF4 – 3FF6 H	More Module Options Register	3E86 – 3E87 H
Last Block Register	3FF2 – 3FF3 H	Module Options Register	3E84 – 3E85 H
Reserved	3FEB – 3FF1 H	Reserved	3E81 – 3E83 H
Mode Code Control Register	3FEA H	Firmware Revision Register	3E80 H
Broadcast Control Register	3FE8 – 3FE9 H	Message Block Area	0000 – 3FE7 H

Figure 4-8 Bus Monitor Look-up Table Mode Memory Map for PCI[e] Carrier Boards

1. 1760 Option only

Reserved	700C – FFFF H	Broadcast Control Register	3FE8 – 3FE9 H
Time Tag (Hi)	700A – 700B H	Reserved	3F80 – 3FE7 H
Time Tag (Lo)	7008 – 7009 H	1760 Header Value Transmit Table[1]	3F40 – 3F7F H
Reserved	7007 H	1760 Header Value Receive Table[2]	3F00 – 3F3F H
Time Tag Reset Register	7006 H	1760 Header Exist Table[2]	3EC0 – 3EFF H
Reserved	7003 – 7005 H	Reserved	3EA6 – 3EBF H
Internal Monitor Connect Register	7002 H	Module Time Register (Lo)	3EA4 – 3EA5 H
Reserved	7001 – 7002 H	Module Time Register (Hi)	3EA2 – 3EA3 H
Module Reset Register	7001 H	Serial Number Register	3EA0 – 3EA1 H
Reserved	4800 – 7000 H	Error Counter (Lo)	3E9E – 3E9F H
Data Block Look-up Table (2K × 8)	4000 – 47FF H	Error Counter (Hi)	3E9C – 3E9D H
Module ID Register	3FFF H	Message Counter (Lo)	3E9A – 3E9B H
Module Configuration Register	3FFE H	Message Counter (Hi)	3E98 – 3E99 H
Start Register	3FFD H	Reserved	3E90 – 3E97 H
Module Status Register	3FFC H	Monitor Response Time Register	3E8E – 3E8F H
Message Status Register	3FFB H	1553A Register	3E8C – 3E8D H
Interrupt Condition Register	3FFA H	Reserved	3E8A – 3E8B H
Reserved	3FF7 – 3FF9 H	Clear Time Tag on Sync Register	3E88 – 3E89 H
Time Tag Resolution Register	3FF6 H	More Module Options Register	3E86 – 3E87 H
Reserved	3FF4 – 3FF5 H	Module Options Register	3E84 – 3E85 H
Last Block Register	3FF2 – 3FF3 H	Reserved	3E82 – 3E83 H
Reserved	3FEC – 3FF1 H	Firmware Revision Register	3E81 H
Mode Code Control Register	3FEB H	Reserved	3E80 H
Reserved	3FEA H	Message Block Area	0000 – 3FE7 H

Figure 4-9 Bus Monitor Look-up Table Mode Memory Map for VME/VXI Carrier Boards

1. 1760 Option only

4.6 Look-up Table Mode

In Look-up Table mode, the module can store 128 unique messages by using a 2K × 8 Look-up Table in dual-port RAM. Each byte in the table is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0 – 127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition register must also be programmed.

Bit	Description
07	1 Interrupt Select bit is enabled
00 – 06	Block Numbers (0 – 127)

Look-up Table Byte Structure

When a 1553 message is received, the Command Word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the Look-up Table. This index is used to extract the Data Block number from the Look-up Table.

	11 most significant bits of the 1553 Command Word					
Base Address	**RT address (5 bits)**	**T/R (1 bit)**	**Sub-address (5 bits)**	**Look-up table (2K x 8)**	**Data Block Storage Area**	**Address of Data Block**
4000+	11111	1	11111	Block #	Data Block 127	27B0 H
	•	•	•	•	•	•
	•	•	•	•	•	•
	•	•	•	•	•	•
4000+	00000	0	00011	Block #	Data Block 3	00F0 H
4000+	00000	0	00010	Block #	Data Block 2	00A0 H
4000+	00000	0	00001	Block #	Data Block 1	0050 H
4000+	00000	0	00000	Block #	Data Block 0	0000 H

Figure 4-10 Look-up Table

To create the address to the table:

1. Isolate the eleven (most significant) bits of the 1553 Command Word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a Data Block for a 1553 receive message to RT#5, Subaddress #3.

RT Address #5			T/R #0 (Rcv)				Subaddress #3				
0	0	1	0	1	0	0	0	0	1	1	LSB

Hex representation = 143 (H)

2. Add the hex value of this part of the Command Word to the base address of the Look-up table (4000 H).

4000	(H)
+ 143	(H)
4143	(H)

3. Write the Data Block number to this location.

Example: **`POKE&H4143`**, writes an 8-bit Block number value to the Look-up table address **`&H14143`**. Each Data Block, beginning at address 0000 is 80 bytes long (for up to 32 1553 Data words). The address of a block is obtained by multiplying its block number by 50 (H).

The block addresses are calculated as follows:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- The location of the block is obtained by multiplying the block number by 50 (H).

To identify the location of the current, or last, 1553 message, use the Last Block register. The Last Block register is updated at the end of each message reception. See **4.13.16 Last Block Register** on page 4-29.

4.6.1 Look-up Table Mode Message Block Area

Information is stored in the memory in the following sequence:	**Byte Offset**
See **Appendix B MIL-STD-1553 Message Formats** on page B-1	• • • •
1553 Command Word	+6
Time Tag (Hi)	+4
Time Tag (Lo)	+2
Message Status Word	0

Figure 4-11 Look-up Table Mode Operation

4.7 Message Status Word

The Message Status Word is identical for all Bus Monitor modes. The Message Status Word indicates the status of the message transfer. The module creates this Word. Do not confuse it with the 1553 Status Word. (See **2.11.44 1553 RT Status Word Table on page 2-38**.) The contents of the Message Status Word are:

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15</td><td>End of Message</td><td>Message transfer completed.</td></tr>
<tr><td>14</td><td>Trigger Found</td><td>Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes:
Store After mode: the Trigger Found bit will be set only in the first Trigger message.
Store Only mode: the Trigger Found bit will be set in every Trigger message. (See 4.10 Trigger Operation on page 4-17)</td></tr>
<tr><td>13</td><td>RT-RT</td><td>RT-to-RT message was received.</td></tr>
<tr><td>12</td><td>Message Error Bit</td><td>Message Error bit (Bit 10) in the RT Status Word was set.</td></tr>
<tr><td>11</td><td>RT Status Bit</td><td>A bit other than the Message Error bit in the RT Status Word was set. The Error Bit is not set in conjunction with this bit.</td></tr>
<tr><td>10</td><td>Bad RT2RT Format</td><td>either Second Command Word in an RT-to-RT message is not a transmit command
or Missing Gap following Second Command Word in an RT-to-RT message</td></tr>
<tr><td>09</td><td>Checksum Error</td><td>The calculated checksum (on the incoming message) does not match when checked against the last Data Word received.
(See 4.9 1760 Option on page 4-16.)</td></tr>
<tr><td>08</td><td>Bus A / B</td><td>Bus on which the message was transferred:
0 = Bus B
1 = Bus A</td></tr>
<tr><td>07</td><td>Invalid Word Received</td><td>At least one invalid 1553 Word received (i.e. bit count, Manchester code, parity).</td></tr>
<tr><td>05 – 06</td><td>Word Count/ Header Error</td><td><table>
<tr><th>Bit 06</th><th>Bit 05</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Word Count Low</td></tr>
<tr><td>1</td><td>0</td><td>Word Count High</td></tr>
<tr><td>1</td><td>1</td><td>1760 Header Error – Header Word received does not match the value set in the Header Value Table.</td></tr>
</table></td></tr>
<tr><td>04</td><td>Incorrect RT Address</td><td>Received 1553 Status Word did not contain the correct RT address.</td></tr>
<tr><td>03</td><td>Incorrect Sync Received</td><td>Sync of either the Status or the Data Word(s) is incorrect.</td></tr>
<tr><td>02</td><td>Non-Contiguous Data</td><td>Invalid gap between received 1553 Words.</td></tr>
<tr><td>01</td><td>Response Time Error</td><td>Response Time error occurred in the message.</td></tr>
<tr><td>00</td><td>Error</td><td>Error occurred. (The error type is defined in one of the other message status bit locations.)</td></tr>
</table>

Message Status Word

Note:

- The Message Status Word is valid only when Bit 15, End of Message, is turned on.
- When the module completes receiving a message over the bus, it writes the Message Status Word for this message in its message storage location. The module then zeros out the Message Status Word in the next message storage location, in preparation for receiving the next message over the bus.

4.8 Time Tag Word

In all Bus Monitor modes, each incoming message is stored with a Time Tag value. The Time Tag value is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon power-up or a software reset and starts counting. When it reaches the value of FFFF FFFF (H) the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset register. (See **4.13.2 Time Tag Reset Register** on page 4-24.)

The Time Tag value can be used to determine the time elapsed between 1553 messages. The equation to determine the Time Tag resolution = (Time Tag Resolution register value + 1) × 4 μsec.

The Time Tag counter's value is written to the dual-port RAM during the reception of the (first) command of each message.

Note: In addition to reading the Time Tag value in the message stack, you can also read the counter's value at any time in the Time Tag counter. See **4.13.1 Time Tag Hi & Lo** on page 4-24.

4.9 1760 Option

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default module setting, or another value the user enters in the 1760 Header Value Transmit/ Receive Table.

See **4.13.19 1760 Header Value Transmit Table**, **4.13.20 1760 Header Value Receive Table** and **4.13.21 1760 Header Exist Table** on page 4-30.

4.10 Trigger Operation

Triggers are supported only in Sequential Fixed-Block mode

A trigger is a filter that the user can set to tell the module when and how to store 1553 messages. The module can be programmed to store messages in the following ways:

Trigger Action:

Store All	Stores all 1553 messages, without regard to triggers; no triggers are active
Store Only	Stores only messages that meet the trigger condition
Store After	Stores only the trigger message and messages that come after the trigger message

Triggering is done based on a **Trigger Source**. The possible sources are:

- **1553 Command Word**
- **Message Status Word**

One or two triggers may be defined. Each trigger specifies a condition of the trigger source, which if it is fulfilled, will cause the **Trigger Action** to occur. Only one trigger source can be defined for the two triggers.

When two triggers are specified, if *either* of the trigger conditions is true, the trigger action will occur. Each trigger is defined using two registers:

- **Trigger Word Registers (1 and 2)**
- **Trigger Mask Registers (1 and 2)**

Use the Trigger Word register to define a particular 1553 Command Word or a Message Status Word as a trigger. For example, the user can use the Message Status Word as the trigger source to store all messages on bus A, only messages with errors, or messages with errors received over bus B, etc. See **4.10.1 Trigger Word Registers (1 and 2)** on page 4-18.

The Trigger Mask register defines which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored (‘don’t care’). The Trigger Mask registers must be defined when using the trigger function. See **4.10.2 Trigger Mask Registers (1 and 2)** on page 4-19.

Set the Trigger Control register to specify the following trigger conditions:

- Trigger source (1553 Command Word or Message Status Word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

See **4.10.3 Trigger Control Register** on page 4-20.

The Trigger Word, Trigger Mask and Trigger Control registers must be set before issuing a Start command to the module. To modify these registers, set the Initialize bit in the Start register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command 81 (H).

4.10.1 Trigger Word Registers (1 and 2)

Address: Word 1 3FF2 – 3FF3 (H)
Word 2 3FEE – 3FEF (H)

Use the Trigger Word register to define a particular 1553 Command Word or a Message Status Word as a trigger. Load these locations (illustrated below) with the desired 1553 Command Word or Message Status Word, which will be used as the trigger source.

The user must also define the Trigger Mask registers when using the trigger function:

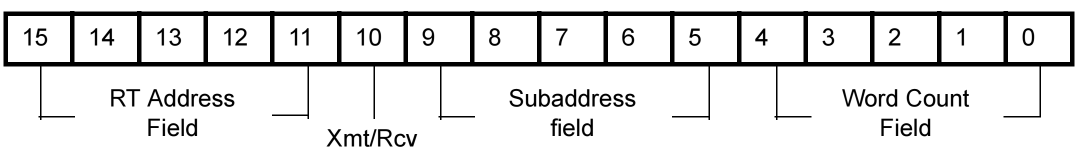
For:	**Define:**
Trigger Word 1 (3FF2 – 3FF3 H)	Trigger Mask 1 (3FF0 – 3FF1 H)
Trigger Word 2 (3FEE – 3FEF H)	Trigger Mask 2 (3FEC – 3FED H)

See **4.10.2 Trigger Mask Registers (1 and 2)** on page 4-19.

To define which trigger is to be active (Trigger #1, Trigger #2, or both) use the Trigger Control register. (See **4.10.3 Trigger Control Register** on page 4-20.)

4.10.1.1 Using the 1553 Command Word: Trigger Word Registers

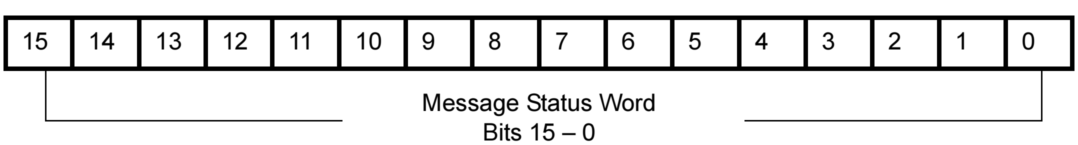
Use a 1553 Command Word as a trigger when it is necessary to filter messages based on information found in the Command Word. For example, to filter messages from a particular RT, or with a particular Word Count, set the Trigger Word register with those parameters defined in the 1553 Command Word.



4.10.1.2 Using the Message Status Word: Trigger Word Registers

Use a Message Status Word as a trigger when it is necessary to filter messages based on information found in the Message Status Word. Do not confuse the Message Status Word with the 1553 Status Word. (See **2.11.44 1553 RT Status Word Table on page 2-38**.) To filter messages transferred over bus A (vs. bus B), or error messages, set the Trigger Word register with those parameters defined in the Message Status Word.

For an explanation see **4.7 Message Status Word** on page 4-15.



4.10.2 Trigger Mask Registers (1 and 2)

Address: **Word 1 3FF0 – 3FF1 (H)**
Word 2 3FEC – 3FED (H)

Set the Trigger Mask register to define which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ("don't care"). The Trigger Mask registers must be defined when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command Word or Message Status Word.

4.10.2.1 Using the 1553 Command Word: Trigger Mask Registers

After setting the Trigger Word register with a 1553 Command Word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the 1553 Command Word trigger.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT Address Field					Xmt/Rcv	Subaddress field					Word Count Field				

1 = Trigger on corresponding bit value in Trigger Word register
0 = Corresponding bit value in Trigger Word register is "don't care"

4.10.2.2 Using the Message Status Word: Trigger Mask Registers

After setting the Trigger Word register with a Message Status Word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the Message Status Word trigger.

For an explanation see **4.7 Message Status Word** on page 4-15.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Message Status Word Bits 15 – 0															

1 = Trigger on corresponding bit value in Trigger Word register
0 = Corresponding bit value in Trigger Word register is "don't care"

4.10.3 Trigger Control Register

Address: 3FEB (H)

The Trigger Control register is relevant only in Sequential Fixed-Block mode. Set the Trigger Control register to specify the following trigger conditions:

a. Trigger source (1553 Command Word or Message Status Word)
b. Type of storage (Store All, Store Only, or Store After)
c. Active trigger word (Trigger Word #1 and/or #2). If both Trigger Words are active, if either condition a. or b. is met, the trigger will occur.

Note: Logic 1 enables the function.

Bit	Description
07	Trigger Source: 0 = 1553 Command Word 1 = Message Status Word
05 – 06	Reserved
04	1 = Store After
03	1 = Store Only
02	1 = Store All
01	1 = Enable Trigger Word #2
00	1 = Enable Trigger Word #1

Trigger Control Register

Example: Defining a Trigger

Conditions:

- Define the Command Word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word #1 (Disable Trigger word #2).

Procedure:

1. Set Trigger Word #1 register to 0825 (H)
2. Set Trigger Mask #1 register to FFE0 (H)
3. Set Trigger Control register to 09 (H)

Note: To use trigger(s), at least one of the bits Store All, Store Only, or Store After, must be set.

4.11 Interrupts

Interrupts are supported in all three Bus Monitor modes.

4.11.1 Sequential Fixed-Block Mode

There are various options for setting interrupts in Sequential Fixed-Block mode, depending on the values set in the Interrupt Condition register (see **4.13.9 Interrupt Condition Register** on page 4-26):

Bit Description	Bit No.	Set values in	Cause an Interrupt
Trigger Word Received	00	Trigger Word, Mask and Control registers[1]	Depending on the store condition set in the Trigger Control register: Store Only — *Each* time the trigger word is received Store After — For all messages received *after* the *first* time the trigger is received See **4.10.3 Trigger Control Register** on page 4-20.
Message Complete	01		Each time any message is received
Block Trigger Match	02	Block number (0 – 199) in the Block Trigger Value register	Set each time that block is updated (i.e. when the Current Message Block register value equals the Block Trigger Value register. See **4.13.12 Current Message Block Register** on page 4-28 and **4.13.13 Block Trigger Value Register** on page 4-28.)

1. See **4.10 Trigger Operation** on page 4-17.

4.11.2 Linked-List Mode

Set the Interrupt Condition register, Bit 01 (Message Complete). An interrupt will occur each time any message is received. (See **4.13.9 Interrupt Condition Register** on page 4-26.)

4.11.3 Look-up Table Mode

An interrupt may be enabled or disabled for each block number assigned in the Look-up Table. Each byte in the table is divided into a 7-bit block and Interrupt Select bit. Set the Interrupt Select bit for the desired block. In addition, set the Interrupt Condition register, Bit 01 (Message Complete). (See **4.13.9 Interrupt Condition Register** on page 4-26.) This will cause an interrupt each time a message is received by those blocks that have the Interrupt Select bit set.

See **4.6 Look-up Table Mode** on page 4-13.

4.12 Program Examples: Bus Monitor Mode

4.12.0.1 PCI[e] Carrier Boards

Bus Monitor Sequential Fixed-Block Mode for PCI[e] Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFF,08`	Set the Module Configuration register for Bus Monitor Sequential Fixed-block mode
`20 POKE &H3FF0,xx`	Set trigger mask #1- low to xx
`30 POKE &H3FF1,xx`	Set trigger mask #1- high to xx
`40 POKE &H3FF2,xx`	Set trigger word #1- low to xx
`50 POKE &H3FF3,xx`	Set trigger word #1- high to xx
`60 POKE &H3FEB,xx`	Set the Trigger Control register (See **4.10.3 Trigger Control Register** on page 4-20.)
`70 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29.)
`80 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = regular (See **4.13.18 Broadcast Control Register** on page 4-29.)
`90 POKE &H3FFC,01`	Start command Messages are read starting from address 0000.

Bus Monitor Sequential Linked-List Mode for PCI[e] Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H10`	Set the Module Configuration register to Bus Monitor Linked-List mode (See **4.13.5 Module Configuration Register** on page 4-25.)
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29.)
`30 POKE &H3FE8,01`	Set the Broadcast Control Register to RT31 = Broadcast (See **4.13.18 Broadcast Control Register** on page 4-29.)
`40 POKE &H3FFC,01`	Start command Messages are read starting from address 0000.

Bus Monitor Look-up Table mode for PCI[e] Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H20`	Set the Module Configuration register to Bus Monitor Look-up Table
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29.)
`30 POKE &H3FE8,00`	Set the Broadcast Control register to RT = 31
`40 POKE &H4143,00`	Set a Look-up table entry so that the Command Words with an RTid of RT#5, Receive mode, and Subaddress 3 point to Data Block #0 (See **4.6 Look-up Table Mode** on page 4-13.)
`50 POKE &H4144, 01`	Set a Look-up table entry so that the Command Words with an RTid of RT#5, Receive mode, and Subaddress 4 point to Data Block #1 (See **4.6 Look-up Table Mode** on page 4-13.)
`60 POKE &H3FFC, 01`	Start Command Messages are read starting from the address pointer derived from the Look-up table entry.

4.12.0.2 VME/VXI Carrier Boards

For VME/VXI, the even and odd addresses are swapped (when using byte swapping). For more information, see **1.5 VME/VXI Byte Swapping** on page 1-9.

Bus Monitor Sequential Fixed-Block Mode for VME/VXI Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFE,08`	Set the Module Configuration register for Bus Monitor Sequential Fixed-block mode
`20 POKE &H3FF1,xx`	Set trigger mask #1- low to xx
`30 POKE &H3FF0,xx`	Set trigger mask #1- high to xx
`40 POKE &H3FF3,xx`	Set trigger word #1- low to xx
`50 POKE &H3FF2,xx`	Set trigger word #1- high to xx
`60 POKE &H3FEA,xx`	Set the Trigger Control register (See **4.10.3 Trigger Control Register** on page 4-20.)
`70 POKE &H3FEB,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29)
`80 POKE &H3FE9,00`	Set the Broadcast Control register to RT31 = regular (See **4.13.18 Broadcast Control Register** on page 4-29)
`90 POKE &H3FFD,01`	Start command
	Messages are read starting from address 0000.

Bus Monitor Sequential Linked-List Mode for VME/VXI Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFE,&H10`	Set the Module Configuration register to Bus Monitor Linked-List mode (See **4.13.5 Module Configuration Register** on page 4-25)
`20 POKE &H3FEB,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29)
`30 POKE &H3FE9,01`	Set the Broadcast Control Register to RT31 = Broadcast (See **4.13.18 Broadcast Control Register** on page 4-29)
`40 POKE &H3FFD,01`	Start command
	Messages are read starting from address 0000.

Bus Monitor Look-up Table mode for VME/VXI Carrier Boards

BASIC Instruction	Remarks
`10 POKE &H3FFE,&H20`	Set the Module Configuration register to Bus Monitor Look-up Table
`20 POKE &H3FEB,00`	Set the Mode Code Control register to 1s and 0s (See **4.13.17 Mode Code Control Register** on page 4-29)
`30 POKE &H3FE9,00`	Set the Broadcast Control register to RT = 31
`40 POKE &H4142,00`	Set a Look-up table entry so that the Command Words with an RTid of RT#5, Receive mode, and Subaddress 3 point to Data Block #0 (See **4.6 Look-up Table Mode** on page 4-13)
`50 POKE &H4145, 01`	Set a Look-up table entry so that the Command Words with an RTid of RT#5, Receive mode, and Subaddress 4 point to Data Block #1 (See **4.6 Look-up Table Mode** on page 4-13)
`60 POKE &H3FFD, 01`	Start Command
	Messages are read starting from the address pointer derived from the Look-up table entry.

4.13 Control Register Definitions

4.13.1 Time Tag Hi & Lo

Address: 700A – 700B (H)
7008 – 7009 (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon a power up or a software reset and starts counting. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

The counter must be read in the following sequence:

1. Read 7008 H – Lo word (16 bit, read only)
2. Read 700A H – Hi word (16 bit, read only)

The Time Tag Resolution register sets the resolution of the counter.

To calculate elapsed time between Time Tags:

Example:

1. The Time Tag Resolution register is set to 0. See **4.13.11 Time Tag Resolution Register** on page 4-27.
2. Calculate the Time Tag Resolution:
   (Time Tag resolution register value + 1) × 4 = (0 + 1) × 4 = 4 µsec
3. Calculate difference between Time Tags:
   150 (Time Tag 2) – 50 (Time Tag 1) = 100
4. Elapsed time
   100 × 4 = 400 µsec

4.13.2 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset register to reset the module Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

4.13.3 Internal Monitor Connect Register — Address: 7003 (H)

Write only For a module in module location 1, if Bit 01 in the Internal Monitor Connect register is set, the module can be used to monitor the module in module location 0, without attaching module 1 to the bus. This also applies to module location 3 which can monitor module 2, and so on.

The Internal Monitor Connect register is reset at power-up (all bits set to 0) or by a module reset.

Bit	Description
02 – 07	Set to 0
01	1 = Monitors the paired module. 0 = Normal monitor.
00	Set to 0

Internal Monitor Connect Register

Note: The Internal Monitor Connect register is reset at power-up (all bits set to 0) or by a module reset.

4.13.4 Module Reset Register — Address: 7000 (H)

Write any value to the Module Reset register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, Module ID and Firmware Revision registers are written by the module after the reset operation is completed.

4.13.5 Module Configuration Register — Address: 3FFF (H)

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration register. To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command. (See **4.13.8 Start Register** on page 4-26.)

Hex Value	Operating Mode
08	Bus Monitor Sequential Fixed -block
10	Bus Monitor Sequential Linked-List
20	Bus Monitor Look-up table

Module Configuration Register Values: Monitor Mode

4.13.6 Module ID Register — Address: 3FFE (H)

The Module ID register contains a fixed value that can be read by your initialization routine to detect the presence of the module. The one-byte value of this register is: 45 (H), ASCII value E.

4.13.7 Module Status Register

Address: 3FFD (H)

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Always set
05 – 06	Indeterminate
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit in the Start register is cleared. Following this, the module sets Bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

4.13.8 Start Register

Address: 3FFC (H)

The Start register controls the Start/Halt operation of the module.

Bit	Bit Name	Description
01 – 07	Reserved	Set to 0
00	Start/Halt	1 = Start Operation 0 = Halt Operation

Start Register

Note: The user can start the module externally by sending a minimum LVTTL pulse of 100 nsec. to the EXSTARTn pin. See **7.4.2 Module Terminal Stick Pin Assignments** on page 7-4.

4.13.9 Interrupt Condition Register

Address: 3FFB (H)

Set the Interrupt Condition register to enable interrupt triggers. When a condition enabled in this register occurs, an interrupt is generated. Logic 1 enables the interrupt condition. Check the Message Status register to determine which condition caused the interrupt. (See **4.13.10 Message Status Register** on page 4-27.)

The Interrupt Condition register must be set before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, then issue a Start command (See **4.13.8 Start Register** on page 4-26.)

Note: For all interrupt conditions, the interrupt will be sent at the end of the message.

Bit	Description
03 – 07	0
02	1 = Block Trigger Match (valid only in Sequential Fixed-Block mode)
01	1 = Message complete (valid in all modes)
00	1 = Trigger Word Received (valid only in Sequential Fixed-Block mode)

Interrupt Condition Register

4.13.10 Message Status Register — Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. Each status bit is described in the table below. Logic 1 indicates that the condition is activated.

Bit	Description
03 – 07	0
02	1 = Block Trigger Match
01	1 = Message Reception In Progress
00	1 = Trigger Word Received – Sequential Fixed-block mode *or* Trigger Word Busy – Linked-List and Look-up table mode The busy bit is set when the module is processing a message. It is set together with message reception in progress, but is reset approximately 5 msec. after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages.

Message Status Register

Note: Status bits are not reset by the module. They must be reset after reading them.

4.13.11 Time Tag Resolution Register — Address: 3FF7 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 μsec.

To determine the Time Tag Counter's resolution, use the following equation:

= (Time Tag Resolution register value + 1) × 4 μsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the module. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command. (See **4.13.8 Start Register** on page 4-26.)

4.13.12 Current Message Block Register — Address: 3FF5 (H)

Sequential Fixed-Block mode only

Read the Current Message Block register to determine the Current Message Block number (0 – 199). The value is incremented by the module as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status Word of the *first* Message block. The End of Message bit (Bit 15) in the Message Status Word will be set.

Note: When Expanded Monitor mode or Enhanced Monitor mode is enabled, the **4.13.22 Expanded Current Message Block Register** register is used instead of this register.

4.13.13 Block Trigger Value Register — Address: 3FF4 (H)

Sequential Fixed-Block mode only

Set the Block Trigger Value register to a block number (0 – 199). This will set a bit in the Message Status register each time that a block is updated, i.e. when the Current Message Block value equals the Block Trigger Value register. It will also cause an interrupt each time that block is updated if in the Interrupt Condition register Bit 02 (Block Trigger Match) is set. (See **4.13.9 Interrupt Condition Register** on page 4-26.)

Set the Block Trigger Value register before issuing a Start command to the module. To modify the Block Trigger Value register, issue a Stop command, modify the register, and then issue a Start command. (See **4.13.8 Start Register** on page 4-26.)

4.13.14 End Buffer Pointer — Address: 3FF4 – 3FF5 (H)

Linked-List mode only

The End Buffer pointer points to the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area. The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H).

4.13.15 Next Message Pointer — Address: 3FF2 – 3FF3 (H)

Linked-List mode only

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

4.13.16 Last Block Register — Address: 3FF2 – 3FF3 (H)

Look-up Table mode only

Read the Last Block register to determine the (Look-up Table) block number of the current 1553 message. This register is used to identify the location of the current 1553 message. The Last Block register is updated at the end of each message reception.

4.13.17 Mode Code Control Register — Address: 3FEA (H)

Set the Mode Code Control register to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

The Mode Code Control register must be set before issuing a Start command to the module. To modify the Mode Code Control register, issue a Stop command, modify the register, then issue a Start command. (See **4.13.8 Start Register** on page 4-26.)

Bit	Description		
02 – 07	0		
00 – 01	**Bit 01**	**Bit 00**	**Subaddresses Recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

4.13.18 Broadcast Control Register — Address: 3FE8 – 3FE9 (H)

Set the Broadcast Control register to specify whether RT address 11111 should be regarded as a valid RT number or as the Broadcast address.

Bit	Description
01 – 07	0
00	1 = RT #31 is Broadcast Address 0 = RT #31 is Regular RT

Broadcast Control Register

4.13.19 1760 Header Value Transmit Table — Address: 3F40 – 3F7F H

1760 Option only

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message. The monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header error** bit is set in the Message Status Word, see **4.7 Message Status Word** on page 4-15.

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

Transmit Subaddress	Header Value	Address
1	**0421 H**	3F42 H
11	**0420 H**	3F56 H
14	**0423 H**	3F5C H

Predefined 1760 Transmit Header Value

4.13.20 1760 Header Value Receive Table — Address: 3F00 – 3F3F (H)

1760 Option only

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. The monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header error** bit is set in the Message Status Word, see **4.7 Message Status Word** on page 4-15.

The 1760 option provides predefined values, and these are preset on each module. The user can change the preset values.

Receive Subaddress	Header Value	Address
11	**0400 H**	3F16 H
14	**0422 H**	3F1C H

Predefined 1760 Receive Header Values

4.13.21 1760 Header Exist Table — Address: 3EC0 – 3EFF (H)

1760 Option only

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for messages directed to that subaddress. In Bus Monitor mode, there is a separate bit to select Header Words for transmit and receive messages.

For those Header Exist table entries for which MIL-STD 1760 provides predefined values, the corresponding Header Exist table entries are preset on each module. To set other values, enable the Header Exist table entry for this Subaddress (set it to 1) and write the value to the Header Value (Transmit/ Receive) table.

Bit	Description
09 – 15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC or RT-to-RT) 0 = Module should not expect a Header word in a transmit message
01 – 07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should not expect a Header word in a receive message

1760 Header Exist Table

Associated Subaddress	Header Value	Address
11	0100 H	**3EC2 H**
14	0101 H	**3ED6 H**
1	0101 H	**3EDC H**

Predefined 1760 Header Values

4.13.22 Expanded Current Message Block Register

Address: 3EBE – 3EBF (H)

Sequential Fixed-Block mode only

When Expanded Monitor mode or Enhanced Monitor mode is enabled, read the Expanded Current Message Block register to determine the Current Message Block number (0 – 799 when Expanded Monitor mode is enabled; 0 – 399 when Enhanced Monitor mode is enabled). (For more information on these modes, see **4.4.1 Message Block Fixed-Block Operation** on page 4-7.)

The value of this register is incremented by the module as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status Word of the *first* Message block. The End of Message bit (Bit 15) in the Message Status Word will be set.

Note: When Expanded Monitor mode or Enhanced Monitor mode is enabled, this register is used instead of the **4.13.12 Current Message Block Register.**

4.13.23 Pretrigger Message Counter Lo & Hi

Address: 3EAA – 3EAB (H)
3EA8 – 3EA9 (H)

Sequential Fixed-Block mode only

The Pretrigger Message Counters Lo & Hi keep track of how many messages were received *until* the trigger kicked in. This enables the user to know that there is activity, until the trigger condition is fulfilled, causing the monitor to actually begin monitoring.

4.13.24 Module Time Register Lo & Hi — Address: 3EA4 – 3EA5 (H), 3EA2 – 3EA3 (H)

This register holds the module time value, which is stored in non-volatile flash memory and loaded at power-up. This value can be modified by calling the Set_ModuleTime_Px function. (See the *1553Px Family Software Tools Programmer's Reference*.) The factory default value is FFFF FFFF (H).

4.13.25 Serial Number Register — Address: 3EA0 – 3EA1 (H)

This register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660.

4.13.26 Error Counter Lo & Hi — Address: 3E9E – 3E9F (H), 3E9C – 3E9D (H)

Error Counter is a running 32-bit counter of message errors.

4.13.27 Message Counter Lo & Hi — Address: 3E9A – 3E9B (H), 3E98 – 3E99 (H)

Message Counter is a running 32-bit counter of all messages received.

4.13.28 Monitor Response Time Register — Address: 3E8E – 3E8F (H)

The Monitor Response Time register sets the maximum wait time until the Monitor considers an RT's Status Response valid.

The Monitor Response Time register is measured in microseconds. The default value of the register is 14 µsec, if not set otherwise by the user.

4.13.29 1553A Register — Address: 3E8C – 3F8D H

Set the 1553A register to simulate MIL-STD-1553A protocol. If set to 1553A protocol, Mode Codes are assumed not to have any data.

4.13.30 Module Function Register

Address: 3E8A – 3E8B (H)

Sequential Fixed-Block mode only

The Module Function register is a 16-bit register that specifies whether the module is using Expanded or Enhanced Monitor. For more information, see **4.4.1 Message Block Fixed-Block Operation** on page 4-7.

Bit	Description
02 – 15	Reserved
01	1 = Enhanced Monitor is in use 0 = Enhanced Monitor is not in use
00	1 = Expanded Monitor is in use 0 = Expanded Monitor is not in use

Module Options Register

Note: Do not set both Bit 00 and Bit 01 to 1. Enhanced Monitor and Expanded Monitor cannot be enabled simultaneously.

4.13.31 Clear Time Tag on Sync Register

Address: 3E88 – 3E89 (H)

Write 1 to the lower byte (3E88 H) of the Clear Time Tag on Sync register to indicate that the Module should clear the Time Tag counter (7008 – 700B H) (resets to 0) upon receipt of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Write 1 to the higher byte (3E89 H) of the Clear Time Tag on Sync register to indicate that the module should clear the Time Tag counter (7008 – 700B H) (resets to 0) upon receipt of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

Note: This register setting does not take effect until the module is restarted.

4.13.32 More Module Options Register

Address: 3E86 – 3E87 (H)

Read only

The More Module Options register is a 16-bit register that provides additional module information.

Bit	Description
06 – 15	Reserved
05	1 = Expanded Block mode is available in BC mode 0 = Expanded Block mode is not available in BC mode
04	1 = Enhanced Monitor mode is available in Sequential Fixed-Block Monitor mode 0 = Enhanced Monitor mode is not available in Sequential Fixed-Block Monitor mode
03	1 = Expanded Block mode is available in Sequential Fixed-Block Monitor mode 0 = Expanded Block mode is not available in Sequential Fixed-Block Monitor mode
02	1 = Module is single function (*PxS*) 0 = Module is multifunction (*Px*)
01	1 = Onboard Loopback option is available 0 = Onboard Loopback option is not available
00	1 = Module is only available in Monitor mode 0 = Module is available in all modes

More Module Options Register

4.13.33 Module Options Register

Address: 3E84 – 3E85 (H)

Read only

The Module Options register is a 16-bit register that provides information about the internal processor and firmware.

Bit	Description
15	1 = PxIII
14	Reserved; set to 1
13	1 = Expanded Block mode is in use in RT mode
12	1 = Module is on a removable card (PCMCIA or ExpressCard) 0 = Module is on an add-in board
11	1 = Replay mode is in use (BC mode only)
10	1 = PxII
09	1 = 1760
08	1 = 1553
00 – 07	4D H Always set; indicates Internal Concurrent Monitor

Module Options Register

4.13.34 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the module firmware. The value 18 (H) would read as revision 1.8.

5 Internal Concurrent Monitor

Chapter 5 describes Internal Concurrent Monitor operation:

An Internal Concurrent Monitor operates automatically on each module when the module is started in either RT or BC/RT modes. It operates in Sequential Fixed-Block mode, the 1553 Message blocks are stored in sequential locations in memory. The storing of messages starts at the first block.

5.1 Internal Concurrent Monitor Memory Map

Message Block Area (409 Blocks)	8000 – FFFF H
Internal Concurrent Monitor Next Message Pointer	3E90 – 3E91 H
Module Options Register	3E84 – 3E85 H

Figure 5-1 Internal Concurrent Monitor Memory Map

When Expanded Block mode is set in RT mode, the Internal Concurrent Monitor Message Block area is reduced.

Message Block Area (204 Blocks)	8000 – BFFF H
Internal Concurrent Monitor Next Message Pointer	3E90 – 3E91 H
Module Options Register	3E84 – 3E85 H

Figure 5-2 Internal Concurrent Monitor Memory Map with Expanded Block Mode

5.2 Message Block Area

The message block area is divided into 409 blocks of 80 bytes each (or 204 blocks when using Expanded Block mode in RT mode). The first block starts at address 8000 (H), the second at 8050 (H), the third at 80A0 (H), etc.

Block #408	FFFF H
•	
Block #203	BFFF H (End of Internal Concurrent Monitor when using Expanded Block mode in RT mode)
•	
Block #2	80A0 H
Block #1	8050 H
Block #0	8000 H

Message Block Area

5.2.1 Message Block Structure

Each message block occupies 40 words. These 40 words include a Message Status Word, 2 consecutive Time Tag words and all the 1553 message words. (See **Appendix B MIL-STD-1553 Message Formats** on page B-1.)

Word 40 is a serial counter. The first message will have a serial counter value of 1; the second message will have a value of 2, etc.

Serial Counter Word
1553 Message Word 36
•
•
1553 Message Word 2
1553 Message Word 1
Time Tag Word #2 (MSB)
Time Tag Word #1 (LSB)
Message Status Word

Internal Concurrent Monitor Message Block Structure

5.2.2 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse it with the 1553 Status Word. (See **2.11.44 1553 RT Status Word Table** on page 2-38.) The contents of the Message Status Word are shown below.

Note: The Message Status Word is different in RT/Concurrent Monitor mode and BC-RT/Internal Concurrent Monitor mode.

A logic 1 indicates the occurrence of a status flag.

Message Status Word: RT/Internal Concurrent Monitor

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed
14	**Bus A / B**	Bus on which the message was transferred (1 = BUS A)
13	**1760 Checksum Error** (1760 option only)	The calculated checksum (on an incoming message) does not match the last Data Word received
12	**Message Error**	Message Error bit (Bit 10) in the RT Status Word was set
11	**RT Status**	A bit other than the Message Error bit in the RT Status Word was set. The Error bit is not set in conjunction with this bit.
10	**TX Time Out**	The module, acting as receiver in RT-to-RT message, did not sense a transmitter Status Word.
09	**Response Error**	Response time error occurred in the message, even if no RT is active on the module.
08	**Invalid Message RT/Internal Concurrent Monitor**	1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT-to-RT message which contains two receive messages.
07	**Invalid Word Received**	At least one invalid 1553 Word received (i.e. bit count, Manchester code, parity)
06	**1760 Header Word Error** (1760 option only)	Header Word received does not match the value set in the Header Value Table (1760 option only) See **2.9.1 Header Word** on page 2-16
05	**Word Count Error**	Incorrect number of words received in the message
04	**Incorrect RT Address**	Received 1553 Status Word did not contain the correct RT address
03	**Sync Error**	Sync of either the Status or the Data Word(s) is incorrect
02	**Non-Contiguous Data**	Invalid gap between received 1553 Words
01	**RT2RT Message**	RT-to-RT message was received
00	**Error**	Error occurred. The error type is defined in one of the other message status bit locations.

Message Status Word: BC-RT/Internal Concurrent Monitor

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed.
14	**Bus A / B**	Bus on which the message was transferred (1 = BUS A)
13	**1760 Checksum Error** (1760 option only)	The calculated checksum (on an incoming message) does not match the last Data Word received. See **3.11.2 Checksum** on page 3-17
12	**Message Error**	Message Error bit (Bit 10) in the RT Status Word was set.
11	**RT Status**	A bit other than the Message Error bit in the RT Status Word was set. The Error bit is not set in conjunction with this bit.
10	**Invalid Message**	1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT- to-RT message which contains two receive messages.
09	**Response Error**	Response time error occurred in the message, even if no RT is active on the module.
08	**1760 Header Word Error** (1760 option only)	Header Word received does not match the value set in the Header Value Table (1760 option only) See **3.11.1 Header Word** on page 3-17
07	**Invalid Word Received**	At least one invalid 1553 Word received (i.e. bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	Received 1553 Status Word did not contain the correct RT address.
03	**Sync Error**	Sync of either the Status or the Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 Words.
01	**RT2RT Message**	RT-to-RT message was received.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Note: The message contents are valid only after the Message Status Word has been written, which is indicated by the End of Message bit being turned on.

5.2.3 1553 Message Words

The 1553 message words are stored in the sequence they appear on the bus, i.e., 1553 Command Words, 1553 Status Words, 1553 Data Words - all according to the order of the specific type of message.

5.3 Control Register Definitions

5.3.1 Internal Concurrent Monitor Next Message Pointer **Address: 3E90 – 3E91 (H)**

The Internal Concurrent Monitor Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The register is updated at the end of each message storage operation. It cycles from 8000 (H) to FFFF (H).

5.3.2 Module Options Register **Address: 3E84 – 3E85 (H)**

Read only

The Module Options register is a 16-bit register that shows information about the internal processor and firmware.

Bit	Description
15	1 = PxIII
14	Reserved – set to 1
13	1 = Expanded Block mode is in use in RT mode
12	1 = Module is on a removable card (PCMCIA or ExpressCard) 0 = Module is on an add-in board
11	1 = Replay mode is in use (BC mode only)
10	1 = PxII
09	1 = 1760
08	1 = 1553
00 – 07	4D H Always set; indicates Internal Concurrent Monitor

Module Options Register

6 Switching Modes of Operation

Many test applications simulate only one mode, for example, Remote Terminal mode. For these applications, this chapter is irrelevant.

If your application requires simulation of more than one mode, you can switch from one mode of operation to another, for example, between the Bus Controller/ Concurrent-RT mode and Remote Terminal modes.

To switch between modes of operation:

1. Halt the operation of the module (via the Start register).
2. Modify the Module Configuration register to the desired mode.

Hex Value	Operating Mode
02	Remote Terminal
04	BC/Concurrent-RT
08	Bus Monitor Sequential Fixed-Block
10	Bus Monitor Sequential Linked-List
20	Bus Monitor Look-Up Table

Module Configuration Register Values

3. Set up the memory as required.
4. Set the Start bit in the Start register.

7 Mechanical and Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the *M4K1553Px* module. The following topics are covered:

7.1 Module Layout

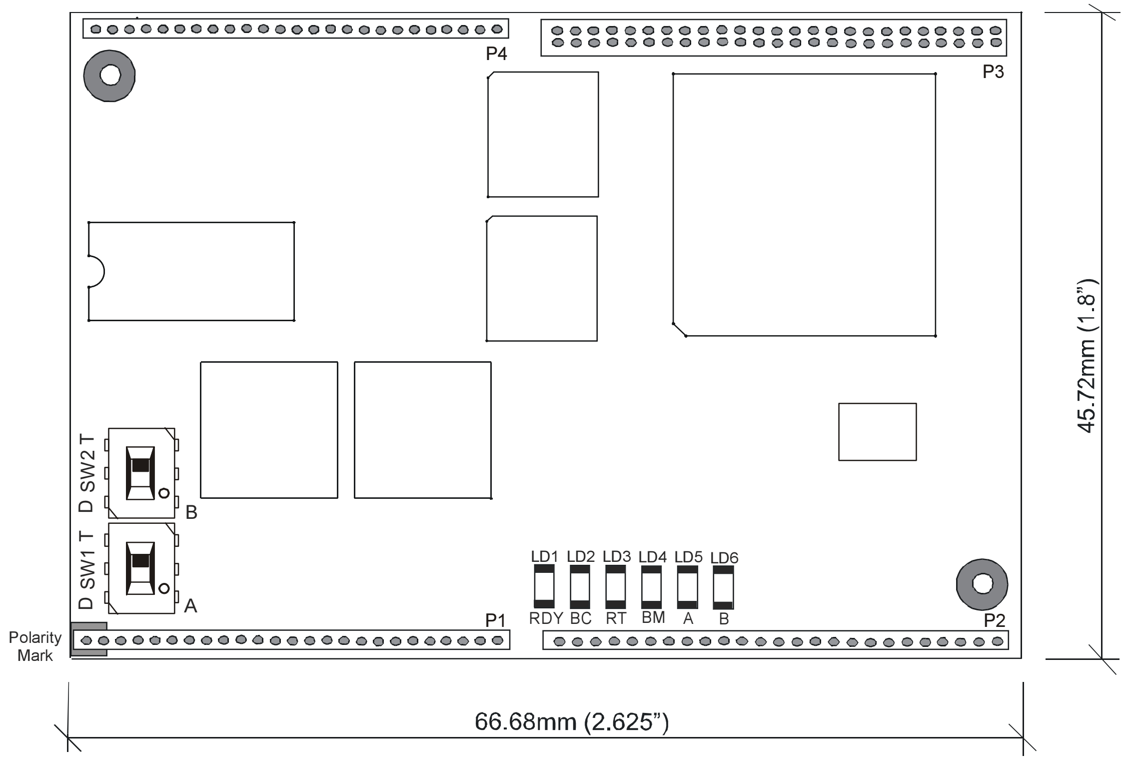


Figure 7-1 *M4K1553Px* Module Layout

7.2 LED Indicators

The *M4K1553Px* module contains six LEDs. The LEDs indicate operational mode and bus activity. The function of each LED is described below:

LED	Indication
LD1	Ready
LD2	BC/Concurrent-RT mode active[1]
LD3	RT mode active[1]
LD4	Monitor mode active[1]
LD5	Bus A active[1]
LD6	Bus B active[1]

Led Indicators

1. Not used on single function module (*PxS*)

7.3 Module Coupling Mode Select DIP Switches

The module can be either Direct Coupled or Transformer Coupled to the 1553 bus. DIP switches are used to select the coupling mode for each bus.

Table 7-1 DIP Switch Settings Required to Select Coupling Mode defines the DIP switch settings:

Coupling Mode	Switch Position
Direct Coupled	At the white marker
Transformer Coupled	Away from the white marker

Table 7-1 DIP Switch Settings Required to Select Coupling Mode

Table 7-2 Bus DIP Switch defines the DIP switch for each Bus:

Bus	DIP Switch
A	SW1
B	SW2

Table 7-2 Bus DIP Switch

Example: To set Bus B to Direct Coupled mode, switch SW2 to the white marker.

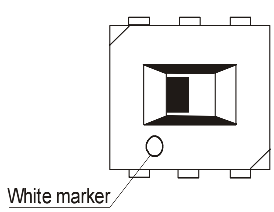


Figure 7-2 DIP Switch: top view

7.3.1 Factory default DIP Switch Settings

The factory default settings are:

DIP Switch	Switch Position	Coupling Mode
SW1 (Bus A)	Away from the white marker	Transformer Coupled
SW2 (Bus B)	Away from the white marker	Transformer Coupled

Table 7-3 Factory Default DIP Switch Settings

7.4 Connectors

The *M4K1553Px* contains four 0.05" spacing strips (P1 – P4) three of which are 25-pin one 50-pin, which comprise a total of 125 pins for all module connections. These pins mate with the carrier board socket strips. Out of these 125 pins, 24 pins are assigned for the communication I/O signals. On the *EXC-4000* carrier board all the module's 24 I/O signals are wired to a 96-pin female connector. This connector is divided into 4 rows (or terminal sticks) of 24 pins each. Each terminal stick is intended for a specific module location. See Figure 7-3.

7.4.1 *EXC-4000* Carrier Board 96-pin Connector

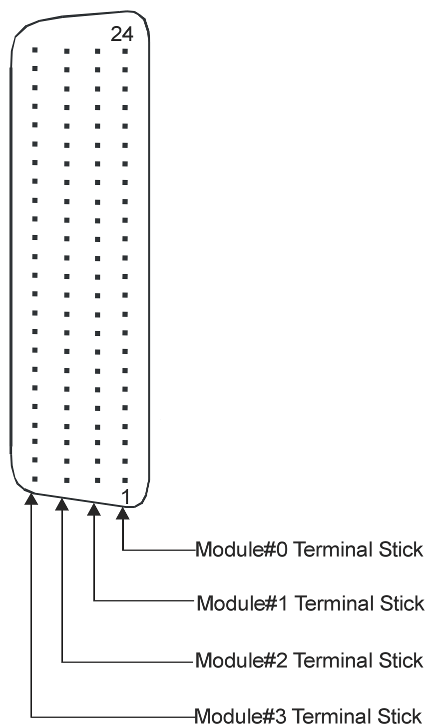


Figure 7-3 *EXC-4000* Carrier Board 96-pin Connector Layout: Front View

7.4.2 Module Terminal Stick Pin Assignments

The following table contains pin assignments for each terminal stick of the *M4K1553Px* module.

	Carrier Board Terminal Stick Pin #	Signal Name	Description
	1	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
	2	BUSALO	Bus A connection Lo
	3	BUSAHI	Bus A connection Hi
	4 – 9	Reserved	
	10	BUSBLO	Bus B connection Lo
	11	BUSBHI	Bus B connection Hi
	12	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
	13	RTA0	Single function module (*PxS*) RT address bit position 0 input[1]
	14	RTA1	Single function module (*PxS*) RT address bit position 1 input[1]
	15	RTA2	Single function module (*PxS*) RT address bit position 2 input[1]
	16	RTA3	Single function module (*PxS*) RT address bit position 3 input[1]
	17	RTA4	Single function module (*PxS*) RT address bit position 4 input[1]
PxS only	**18**	RTPTY	Single function module (*PxS*) RT address parity bit input[1]
	19	RTLOCKn	Single function module (*PxS*) RT address lock 0 = RT number locked (RT address is set to the value represented by pins 13 – 18) 1 = RT number unlocked (RT address can be changed by writing to the RT Number Register)
	20	GND	Provided for single function module (*PxS*) RT address pins that need to be set to '0'
	21 – 22	Reserved	
	23	EXSTARTn	External Start LVTTL input. Provides an option to start the module externally by applying a negative pulse with respect to the GND pin, with a minimum width of 100 nsec. Before applying the pulse, the module should be fully set up in the required mode, except the Start register Bit 00, which should be left at 0. To stop the selected operation, follow the normal procedure described under the Start register.
	24	GND	Provides ground reference for the digital signal connections

***M4K1553Px* Connector Pin Assignment Configuration**

1. Pin shorted to ground = logic 0
   Open = logic 1
   See also **2.11.1 RT Number Register (PxS Only)** on page 2-18

7.4.3 *M4K1553Px* Module Adapter Cable

A standard adapter cable which converts the Molex® terminal stick to two female twinax connectors (Trompeter CJ70 or equivalent) for Bus A and Bus B may be purchased from Excalibur.

The twinax connectors mate, for example, with Trompeter PL75 male twinax connectors. These connectors are not supplied by Excalibur.

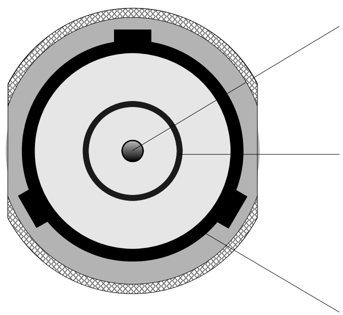


Figure 7-4 Twinax Connector – Front View

7.4.3.1 Adapter Cable Connectors Pin Assignments

	Twinax Conn. Pin Position	Signal Name	Description
Bus A	CENTER PIN	BUSHI	Bus A Connection Hi
	INNER SHEATH	BUSLO	Bus A Connection Lo
	BODY ASSEMBLY	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
Bus B	CENTER PIN	BUSHI	Bus B Connection Hi
	INNER SHEATH	BUSLO	Bus B Connection Lo
	BODY ASSEMBLY	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer

Table 7-4 Adapter Cable Connectors Pin Assignments

For more information refer to **Chapter 8 Ordering Information** and the ordering information in the *EXC-4000* carrier board's *User's Manual*.

7.5 Power Requirements

The *M4K1553Px* power requirements are:

+5V @ 270mA (0% duty cycle: non-transmitting on 1553 bus)

+5V @ 570mA (50% duty cycle: transmitting on 1553 bus))

+5V @ 770mA (100% duty cycle: transmitting on 1553 bus)

+12V @ 15mA

8 Ordering Information

Chapter 8 explains how to indicate which options you want when ordering a *M4K1553Px* module.

Part Number	Option	Description
M4K1553Px		MIL-STD-1553 multifunction interface module for the Excalibur 4000 family of carrier boards. Supports multiple RT, BC/Concurrent -RT and Bus Monitor modes with an Internal Concurrent monitor for RT and BC/RT operation.
M4K1553Px-LB		Same as *M4K1553Px* with an Onboard Loopback option.
M4K1553PxS		Single function version of the *M4K1553Px* module. Supports single RT, BC and Bus Monitor modes with an Internal Concurrent monitor for RT and BC operation; without error injection.
M4K1553PxM		Monitor-only version of the *M4K1553Px* module.
	-E	With extended temperature operation (-40° to +85°C).
	-001	With conformal coating.
	-1760	MIL-STD-1760 version of the module. (Not available for *M4K1553PxM*.)
X4KFx		*M4K1553Px* adapter cable, 0.5 meter length with two twinax female connectors. See **7.4.3 M4K1553Px Module Adapter Cable** on page 7-5.

Note: The Internal Concurrent Monitor (formerly listed as the -M option) is now a standard feature of the *M4K1553Px*.

Appendix A MIL-STD-1553 Word Formats

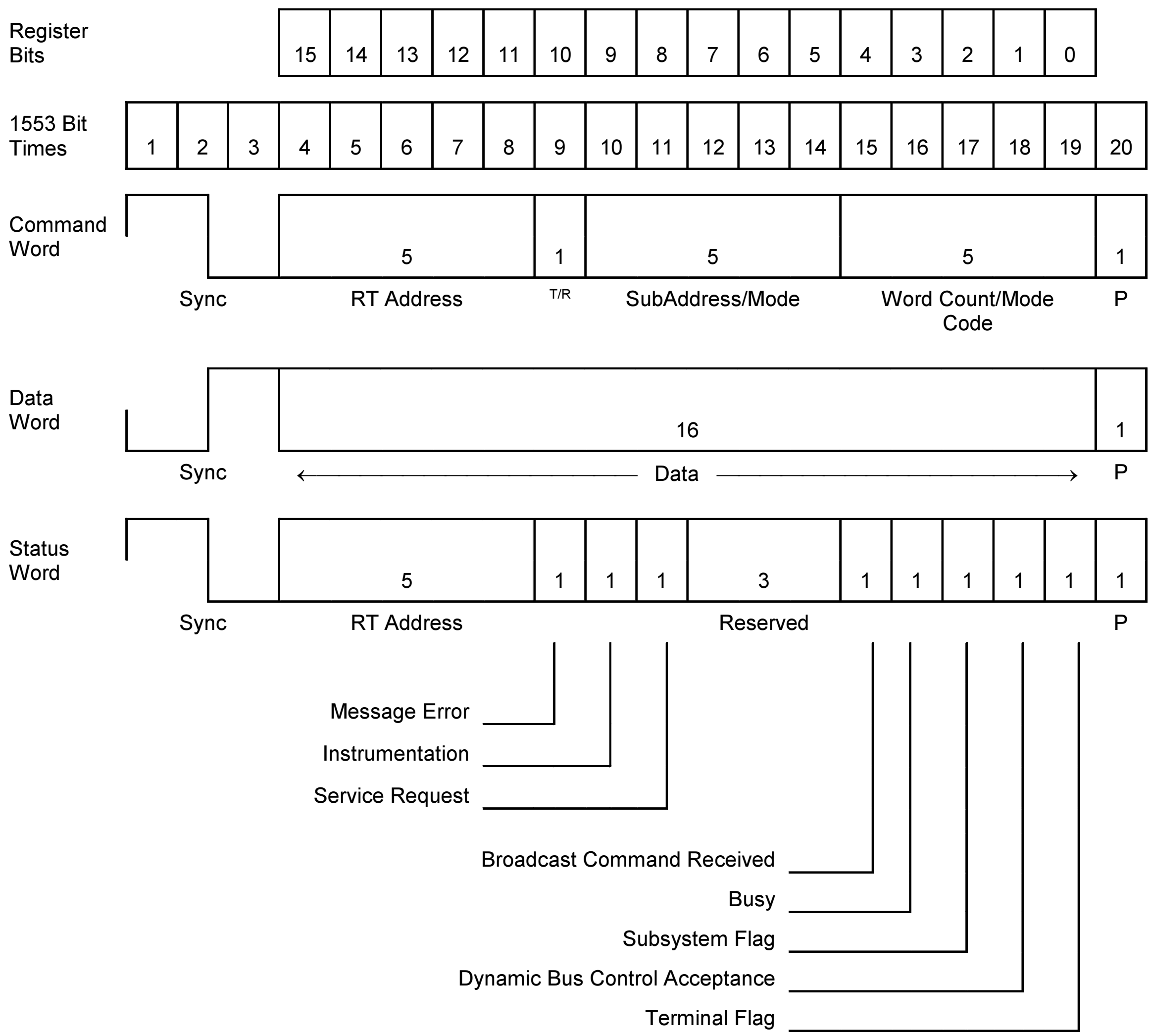


Figure A-1 MIL-STD-1553 Word Formats

Note: T/R = Transmit/Receive
P = Parity

Appendix B MIL-STD-1553 Message Formats

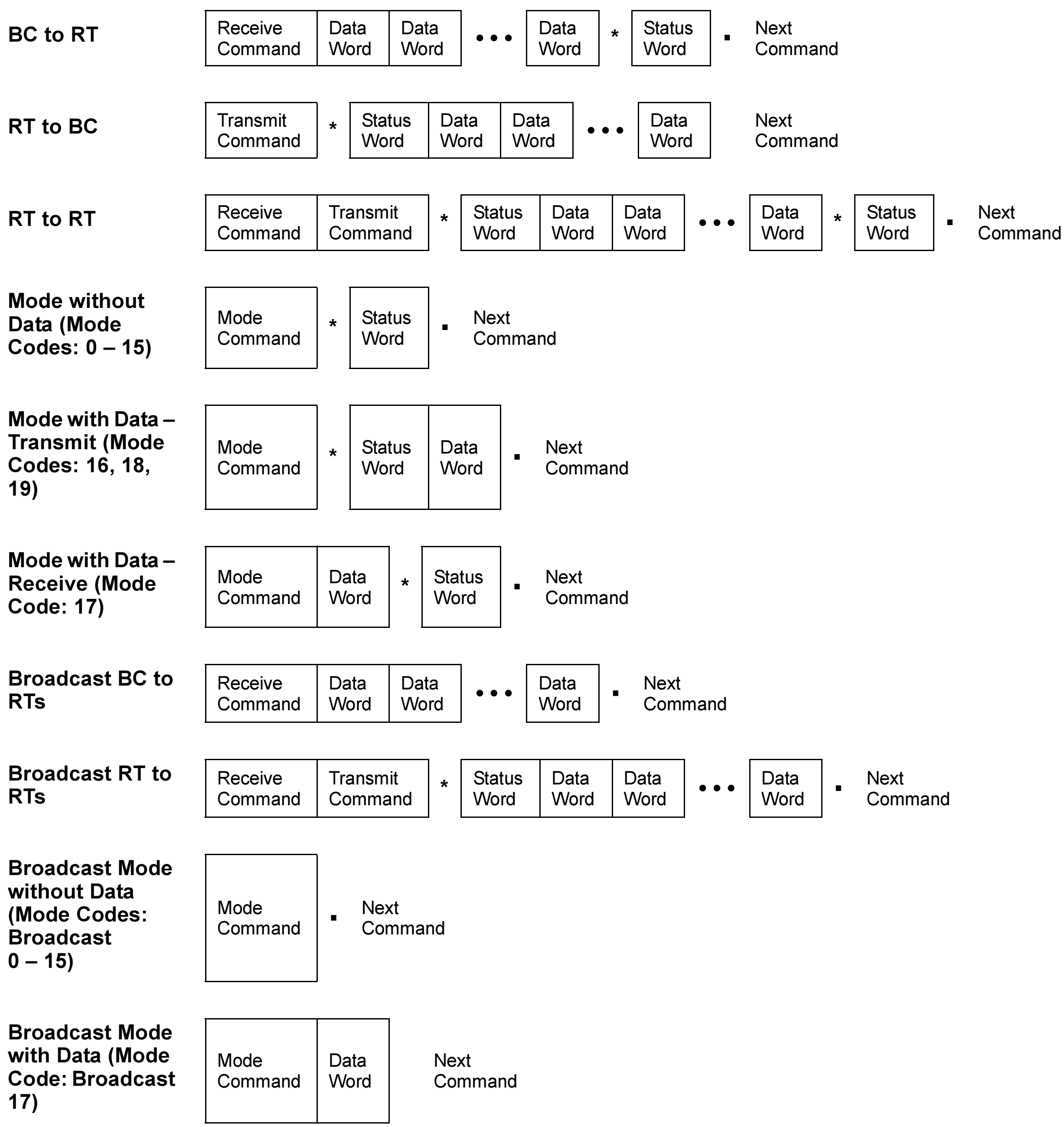


Figure B-1 MIL-STD-1553B Message Formats

Note: * = Response time
▪ = Intermessage Gap time

Appendix C Internal Loopback Test

The Internal Loopback Test is used to check the 1553 front-end logic, excluding transceivers and coupling transformers.

Note: When running a loopback, all values previously written to registers and memory addresses are erased.

To initiate the Internal Loopback Test:

1. Write ED (H) into the Module/Channel Configuration register.
2. Write 1 into the Start register.
3. Wait for 0 in the Start register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

	Definition	Address in Dual-Port RAM	Status Value
{struct I_LOOPBACK			
usint frame_val;		0	X (not for user)
usint frame_status;	frame time counter status	2	8000H passed, 8001H failed
usint resp_status;	response time counter status	4	8000H passed, 8001H failed
usint early_val;		6	6 LSB must be 15H
usint receive_data1;	first looped word test, using command sync	8	5555H
usint status_1;		A	8000H passed, else failed
usint receive_data2;	second looped word test, using data sync	C	AAAAH
usint status_2;		E	8000H passed, else failed
usint mc_status;	mode code function test	10	8000H passed, else failed
usint ttag_val_lo;		12	30D4H ± 2
usint ttag_val_hi;		14	0
usint ttag_status;	time tag status	16	8000H passed, 8001H failed
usint prl;		18	(The CPU version)
} *I_loopback;			

Appendix D External Loopback Test

The External Loopback Test is used to check the 1553 transceivers, transformers and associated bus cables. The External Loopback Test requires a loopback cable to connect bus A to bus B.

Alternatively, on a -LB module you can activate an Onboard Loopback. When using an Onboard Loopback, the signals are looped back before the I/O connectors. Therefore, when an Onboard Loopback is activated, the external wiring and the I/O connector itself are not tested. To activate the Onboard Loopback, use the **Loopback Relay Select Register** on page 3-20.

Note: When running a loopback, all values previously written to registers and memory addresses are erased.

To initiate the External Loopback Test:

1. Write FF (H) into the Module Configuration register.
2. Write 1 into the Start register.
3. Wait for 0 in the Start register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

	Definition/conditions for passing E_loopback test	Address in Dual-Port RAM	Status Value
{struct E_LOOPBACK			
usint frame_val;		0	X (not for user)
usint frame_status;	frame time counter status	2	8000H passed, 8001H failed
usint cmd_send[8];		4	cmd_send[0]: 5555H
	TX-A, RX-B command sync	6	cmd_send[1]:8000H passed, else failed
		8	cmd_send[2]: 1234H
	TX-A, RX-B data sync	A	cmd_send[3]:8000H passed, else failed
		C	cmd_send[4]: 5555H
	TX-B, RX-A command sync	E	cmd_send[5]:8000H passed, else failed
		10	cmd_send[6]: 1234H
	TX-B, RX-A data sync	12	cmd_send[7]:8000H passed, else failed
usint ttag_val_lo		14	30D4H ± 2
usint ttag_val_hi		16	0
usint ttag_status;	time tag status	18	8000H passed, 8001H failed
} *E_loopback;			

For more information on External Loopbacks, see **Appendix E Application of External Loopback Test** on page E-1.

Appendix E Application of External Loopback Test

The External Loopback Test feature of Excalibur Systems' *Px* module requires a particular loopback cable configuration. The External Loopback Test checks the 1553 transceivers, transformers and associated cables when the module is disconnected from the main MIL-STD-1553 bus. With Bus A and Bus B outputs connected together, the function, External_Loopback_Px initiates a special hardware test that transmits Command Sync and Data Sync messages between the two buses.

For proper functioning of the test, a correct stub-to-stub connection must be made. Two methods of properly connecting Bus A and Bus B stubs together are:

- **Direct Coupling**
- **Transformer Coupling**

E.1 Running a Loopback Using Direct Coupling

To use Direct Coupling, set the module's DIP switches to Direct Coupled mode. See **7.3 Module Coupling Mode Select DIP Switches** on page 7-2.

Note: Direct Coupled Stubs are not available for the *EXC-1553ccVME/Px* board.

For stub lengths of less than one foot, the main MIL-STD-1553 bus can be directly coupled. If this coupling method is being employed, then the Direct Coupled Loopback Test Cable, part number MC1003, must be utilized when running the External Loopback Test. The cable provides one Trompeter PL75 (or equivalent) twinax connector on each end and an integrated 39-Ohm termination resistor across the data high and data low lines. To perform the External Loopback Test, disconnect the module's Bus A and Bus B stub connections to the main 1553 bus, connect the test cable to the Bus A and Bus B connections coming from the module and then run the loopback test. When the External Loopback Test is completed, disconnect the test cable and reconnect the module's Bus A and Bus B stubs to the main MIL-STD-1553 bus.

E.2 Running a Loopback Using Transformer Coupling

To use Transformer Coupling, set the module's DIP switches to Transformer Coupled mode. See **7.3 Module Coupling Mode Select DIP Switches** on page 7-2.

This is the preferred method of coupling to the main MIL-STD-1553 bus and requires a bus coupler at the junction of the main bus and stub. If this coupling method is being employed, then the Transformer Coupled Loopback Test Cable, part number ESI-235-1-176-X-XX-XX, must be utilized for running the External Loopback Test. The cable provides one Trompeter PL75 (or equivalent) twinax connector on each end and an integrated two stub internally terminated (39-Ohms) in-line bus coupler. To perform the External Loopback Test, disconnect the board's Bus A and Bus B stub connections to the bus couplers, connect the test cable to the Bus A and Bus B connections coming from the board and then run the loopback test. When the External Loopback Test is completed, disconnect the test cable and reconnect the board's Bus A and Bus B stubs to the bus couplers.

Note: The stub cables may be connected or disconnected with the board powered on but not while the board is transmitting over the bus.

Index

October 2011, Rev C-5