EXC-4500ccVPX

Carrier Board
for VPX Systems

User's Manual

EXCALIBUR SYSTEMS

311 Meacham Ave ♦ Elmont ♦ NY 11003 ♦ tel. (516) 327-0000 ♦ fax (516) 327-4645
e-mail: excalibur@mil-1553.com website: www.mil-1553.com

Table of Contents

Figures

Tables

1 Introduction

1.1 Overview

The *EXC-4500ccVPX* is a 3U multiprotocol conduction cooled VPX interface board for flyable avionics applications. The *EXC-4500ccVPX* has a ruggedized design with a PCI Express interface. It comes with three built-in modules plus an optional fourth module.

- Module 0 is a built-in M4KDiscrete module.
- Module 1 is a built-in M4KSerial module.
- Module 2 is a built-in M4K1553Px module.
- Module 3 can be any of the following:

M4K1553P*x*	MIL-STD-1553 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. Supports an Internal Concurrent Monitor in RT and BC/RT modes.
M4K1553P*x*-1760	Same as M4K1553Px plus MIL-STD-1760 options.
M4K429RT*x*	ARINC 429 multi-channel interface module. This module supports either five or ten ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M4KDiscrete	Discrete I/O interface module. This module supports 20 bi-directional discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M4KSerial	Serial communications interface module. This module supports either two or four independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.
M4KCAN	CAN protocol interface module. This module supports either two, four or six independent channels of CAN 2.0B protocol with standard and extended message frames and message identifiers.
M4K708	ARINC 708 interface module. This module supports two channels of ARINC 708/453, each one selectable as either transmit or receive
M4KMMSI	Mini Munitions Store Interface module. This module supports RT, BC/ Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 8 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and 1 monitor output.

Excalibur will be adding modules to those listed above, increasing the *EXC-4500ccVPX*'s flexibility even further.

1.1.1 *EXC-4500ccVPX* Board Features

General Specifications

EXC-4500ccVPX	A standard VPX board that conforms to: • ANSI/VITA 46.0 VPX Baseline Specification • PCI Express Host Interface (ANSI/VITA 46.4) • ANSI/VITA 48.2 Conduction Cooled Mechanical Specifications (Type 1, 1 in. plug-in thickness)
Supports up to four modules	
Protocols supported:	ARINC 429/575 (5 or 10 channels) ARINC 708/453 MIL-STD-1553 (Px family) MIL-STD-1760 Discrete I/O Serial - RS485/RS422/RS232 CAN MMSI
Timer	16-bit count down timer
Resolution	1 μs min, 65536 μs max
Output	Interrupt, Global reset

Operating Environment

Temperature:	0° – 70°C standard temp. -40° to +85°C extended temp. (optional)
Humidity:	5% – 90% non-condensing

Physical Characteristics

Dimension	160mm – 100mm
Weight	TBD

Host Interface

PCI Express compliance:	PCIe v1.1 x1 lane with DMA support
Memory space occupied:	512 Kbytes (128K per module)
Interrupts:	INTA# virtual wire
Power	Depends on configuration

IRIG B Time Code Input

Carrier wave	1KHz Amplitude modulated sine wave
Rate Designation	100 peaks per second
Modulation ratio	3:1
Input Amplitude	0.8 Vpp min, 3.5 Vpp max, 3 Vpp Typ
Coded Expressions supported	BCD Time-of-Year code word, Control functions, straight binary seconds time-of-day (seconds-of-day)
Application	Synchronization of Time Tags, display and IRIG B time

Software Support

C Drivers with source code
Mystic Windows software for ARINC 429 modules
MerlinPlus Windows software for Px modules
Merlin Windows software for MCH modules
Exalt Plus (Optional - contact your Excalibur representative for details)

1.1.2 *EXC-4500ccVPX* Block Diagram

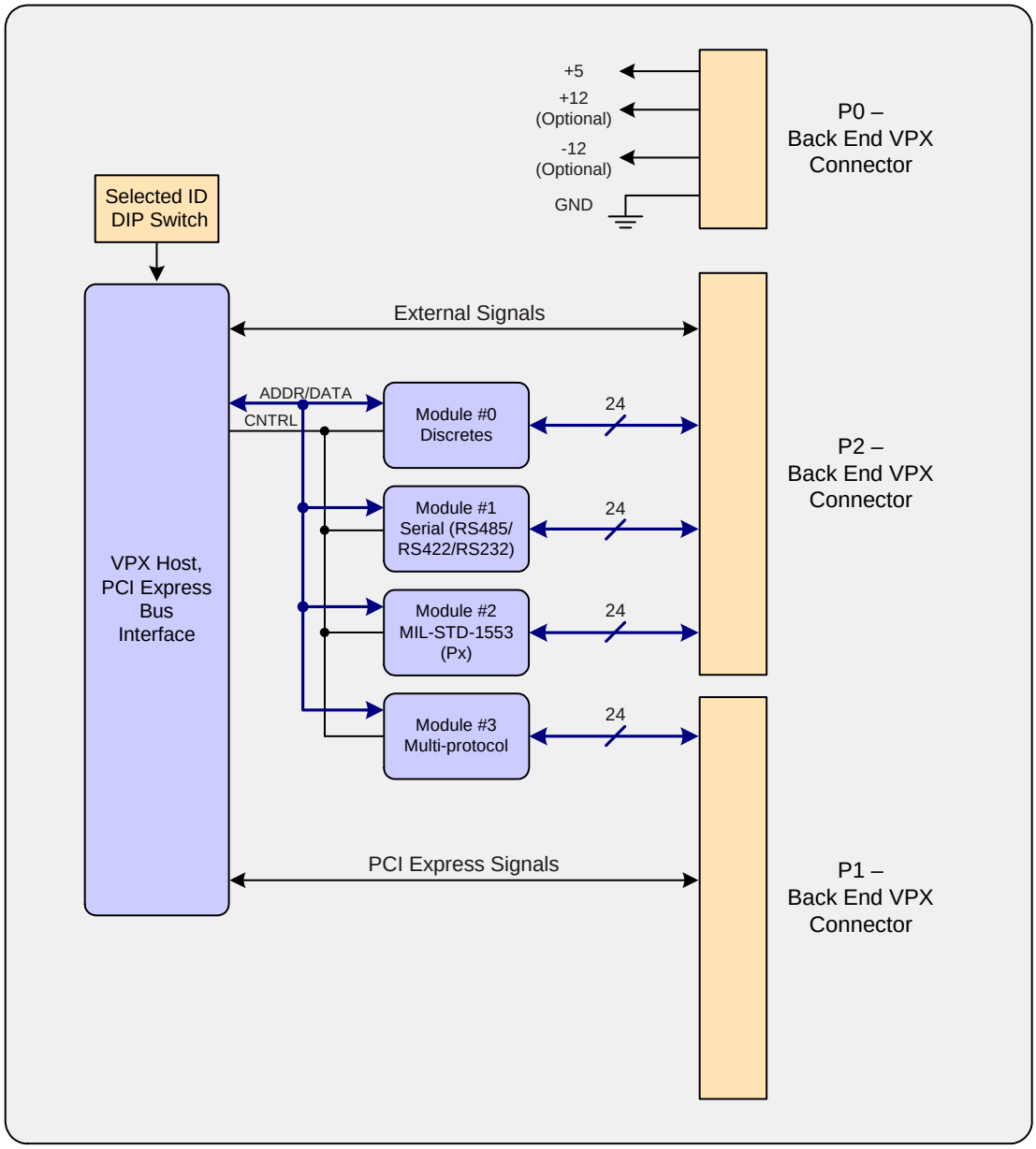

Figure 1-1 *EXC-4500ccVPX* Block Diagram

1.2 Installation

To operate the *EXC-4500ccVPX* board:

1. Install the board in the computer.
2. Add Excalibur Software Tools to the hard disk.

1.2.1 Installing the Board

Installation of the *EXC-4500ccVPX* board is similar to that of all PCI[e] boards. The *EXC-4500ccVPX* complies with the "Plug and Play" specification of the PCI standard. As such, its absolute address is determined by the BIOS at start-up.

Warning: Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.

To install the *EXC-4500ccVPX*:

1. Make certain the computer's power source is disconnected.
2. Insert the board into a VPX back plane slot.
3. Tighten the board's wedge locks to ground the board to the computer.
4. Turn on the power of the VPX system.

   A **Found New Hardware** message appears.
5. Follow the on-screen instructions for your specific operating system and service pack.

1.2.2 Adding Excalibur Software Tools

The standard software included with the *EXC-4500ccVPX* card is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com

For information about adding the accompanying software drivers, see the **`readme.pdf`** file for the *EXC-4500ccVPX* on the *Excalibur Installation CD*.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:

2.1 Memory Structure

The *EXC-4500ccVPX* requests three memory blocks:

- The first memory block (Base 0) is 512 KB in size and contains the memory space for the modules on the board. For more information, see section **2.5 Module Memory Space Map** on page 2-14.
- The second memory block (Base 2) is 4 KB in size and contains the Global Registers. For more information, see section **2.6 EXC-4500ccVPX Global Registers Map** on page 2-15.
- The third memory block (Base 4) is 8 KB in size and contains the DMA Registers. For more information, see section **2.4 DMA Registers for PCI Express** on page 2-10.

2.2 PCI Configuration Space Header

The board includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

31 24	23 16	15 08	07 00	
MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (not used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer – not used = 0s				28 H
Base Address Register #5 – not used				24 H
Base Address Register #4 – DMA Registers				20 H
Base Address Register #3 – Reserved				1C H
Base Address Register #2 – Global Registers				18 H
Base Address Register #1 – Reserved				14 H
Base Address Register #0 – Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H

Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value: E450 H

Size: 16 bits

The Device Identification register contains the board's device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	Always set to 0
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 1
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the *EXC-4500ccVPX* board does not use I/O space, the value of this register is ignored.

Table 2-1 PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	Not used
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 00 (fast timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 0
06	**UDF Supported**	Set to 0
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
03	**Interrupt Status**	This bit is set when an interrupt is received.
00-02	**Reserved**	

Table 2-2 PCI Status Register

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the *EXC-4500ccVPX*.

2.3.6 Class Code Register (CLCD) Address: 09–-0B (H)

Power-up value: FF0000 H

Size: 24 bits

The Class code Register value indicates that the *EXC-4500ccVPX* does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) Address: 0C (H)

Power-up value: 10 H

Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.9 Header Type Register (HDR) Address: 0E (H)

Power-up value: 00 H

Size: 8 bits

The *EXC-4500ccVPX* is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) Address: 0F (H)

Power-up value: 00 H

Size: 8 bits

The Built-In Self-Test register is not implemented in the *EXC-4500ccVPX*.

2.3.11 Base Address Registers (BADR)

Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Three memory pages are required by the board: one for the module memory space, one for the Global Registers and one for the DMA registers.

Register	Offset	Size	Function
Base Address 0	10 H	512 KB	Module memory space
Base Address 2	18 H	4 KB	Global registers
Base Address 4	20 H	8 KB	DMA registers

Table 2-3 Base Address Registers Definition

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

The following table describes the bits of the Base Address Register.

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01-02	Always 2 – memory may be mapped anywhere within the 64 bit memory space
00	Always 0 – indicates memory space

Table 2-4 Base Address Register

2.3.12 Cardbus CIS Pointer

Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the *EXC-4500ccVPX*.

2.3.13 Subsystem ID — Address: 2C (H)

Power-up value: 0000 H

Size: 16 bits

2.3.14 Subvendor ID — Address: 2E (H)

Power-up value: 0000 H

Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM) — Address: 30 (H)

Power-up value: 00000000 H

Size: 32 bits

The Expansion ROM Space is not implemented on the *EXC-4500ccVPX*.

2.3.16 PCI Capabilities Pointer — Address: 34 (H)

Power-up value: 50 H

Size: 8 bits

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process.

2.3.17 Interrupt Line Register (INTLN) — Address: 3C (H)

Power-up value: 00 H

Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) — Address: 3D (H)

Power-up value: 01 H

Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) Address: 3E (H)

Power-up value: 00 H

Size: 8 bits

The Minimum Grant register is not implemented on the *EXC-4500ccVPX*.

2.3.20 Maximum Latency Register (MAXLAT) Address: 3F (H)

Power-up value: 00 H

Size: 8 bits

The Maximum Latency register is not implemented on the *EXC-4500ccVPX*.

2.4 DMA Registers for PCI Express

Direct Memory Access (DMA) enables the board to access a module's memory space for reading and writing independently of the computer's CPU. This results in faster data transfer to and from the board, with much less CPU overhead than when not using DMA.

There are two DMA channels:

- **DMA0** – DMA channel 0 is used for DMA writes
- **DMA1** – DMA channel 1 is used for DMA reads

Reserved		44 – 1FFF (H)
Base Address for DMA0 and DMA1 Transfers		40 H
Reserved		38 H
Reserved (Bits 2 – 31)	DMA Interrupt Status (Bits 0 – 1)	34 H
Reserved		30 H
Reserved		28 H
Reserved		24 H
Reserved		20 H
DMA1 Control		1C H
DMA1 Data Transfer Size		18 H
DMA1 Address of Contiguous Host Memory – High 32 bits		14 H
DMA1 Address of Contiguous Host Memory – Low 32 bits		10 H
DMA0 Control		0C H
DMA0 Data Transfer Size		08 H
DMA0 Address of Contiguous Host Memory – High 32 bits		04 H
DMA0 Address of Contiguous Host Memory – Low 32 bits		00 H

2.4.1 DMA0 Address of Contiguous Host Memory (Low and High)

Address: **00 (H) (Low)**
04 (H) (High)
Length **64 bits**

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data. Upon successful completion of a transfer, this register contains the following value: Start Address + Write Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.4.2 DMA0 Data Transfer Size

Address: 08 (H)
Length 32 bits

This register contains the total amount of data (in bytes) to be written during a DMA write transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA write transfer, the value of this register should be 0.

2.4.3 DMA0 Control Register

Address: 0C (H)
Length 32 bits

This register contains information about, and controls, the DMA write data transfer.

Bit	Description	
12-13	Reserved – set to 0	
08-11	DMA channel state	These bits describe the state of the DMA write channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a module 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) The DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal module memory. 1100 – 1111 = (busy state) Reserved
04-07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00-01	Reserved – set to 0	

Table 2-5 DMA0 Control Register

2.4.4 DMA1 Address of Contiguous Host Memory

Address: 10 (H) (Low)
14 (H) (High)
Length 64 bits

The start address of the Contiguous Host Memory must be written to this register by the user. The address stored in this register is automatically incremented during the process of the DMA transfer. The current value in this register is the address following (the address of) the last requested data.

Upon successful completion of a transfer, this register contains the following value: Start Address + Read Transfer Size, where Start Address is the start address of the Contiguous Host Memory.

2.4.5 DMA1 Data Transfer Size

Address: 18 (H)
Length 32 bits

This register contains the total amount of data (in bytes) to be read during a DMA read transfer. The total transfer size must be written to this register by the user. The transfer size value stored in this register is automatically decremented during the process of the DMA transfer. The current value stored indicates the remaining amount of data that needs to be transferred. Upon successful completion of a DMA read transfer, the value of this register should be 0.

2.4.6 DMA1 Control Register

Address: 1C (H)
Length 32 bits

This register contains information about, and controls, the DMA read data transfer.

Bit	Description	
12-13	Reserved – set to 0	
08-11	DMA channel state	These bits describe the state of the DMA read channel. 0000 = (idle state) Last transfer ended successfully 0001 = (idle state) Last transfer was stopped by a module 0010 = (idle state) Last transfer ended because of CPL timeout 0011 = (idle state) Last transfer ended because of CPL UR error 0100 = (idle state) Last transfer ended because of CPL CA error 0101 – 0111 = (idle state) Reserved 1000 = (busy state) The DMA channel is busy processing 1001 = (busy state) Requesting transfer. The DMA channel is in the process of requesting data from the host computer 1010 = (busy state) The DMA channel is waiting for completion of a read data transfer in response to a DMA read request 1011 = (busy state) Waiting for board to provide/accept data. The DMA channel is waiting for completion of a data transfer to or from the internal module memory. 1100 – 1111 = (busy state) Reserved
04-07	Reserved – set to 0	
03	Abort DMA transfer	1 = Abort transfer 0 = no effect
02	Start DMA transfer	1 = Start DMA transfer 0 = no effect
00-01	Reserved – set to 0	

Table 2-6 DMA1 Control Register

2.4.7 DMA Interrupt Status Register

Address: 34 (H)
Length 2 bits

Bit 0 of this register is set upon completion of a DMA transfer on DMA0 (DMA write). Bit 1 is set upon completion of a DMA transfer on DMA1 (DMA read). To clear either bit, write a 1 to the corresponding location.

Note: The two bits of the DMA Interrupt Status Register work together with the five bits of the Global Interrupt Status Register. When any of these seven bits are set, an interrupt is generated. To locate the source of an interrupt to the host, both of these registers need to be read.

In order to reset an interrupt, you must reset the appropriate bits of **both** the DMA Interrupt Status Register **and** the Global Interrupt Reset Register. See **2.6.3 Interrupt Status Register** on page 2-17.

2.4.8 Base Address for DMA0 and DMA1 Transfers

Address: 40 (H)
Length 32 bits

This register contains the start address of the current DMA transfer (read or write transfer). The base must be written to this register by the user.

2.5 Module Memory Space Map

The module memory space map resides in the first memory block. Each module is allocated a space of 128KB which is mapped as shown in **Figure 2-2 Module Memory Space Map**. For information about the modules, see the user's manual for each module. (The mechanical and electrical specifications for the built-in modules are described in this manual. See Chapter 3 **Mechanical and Electrical Specifications**.)

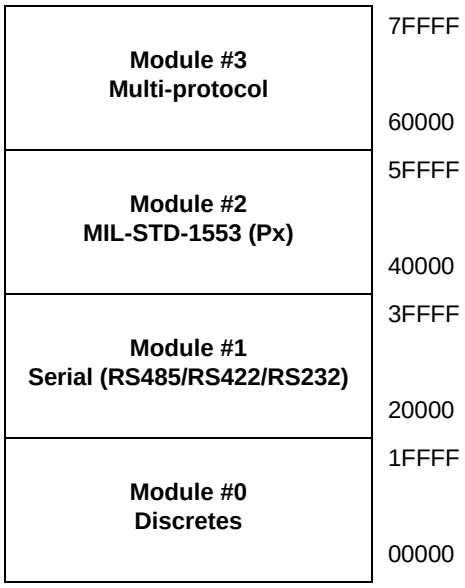

Figure 2-2 Module Memory Space Map

2.6 *EXC-4500ccVPX* Global Registers Map

The board global registers reside in the second memory block.

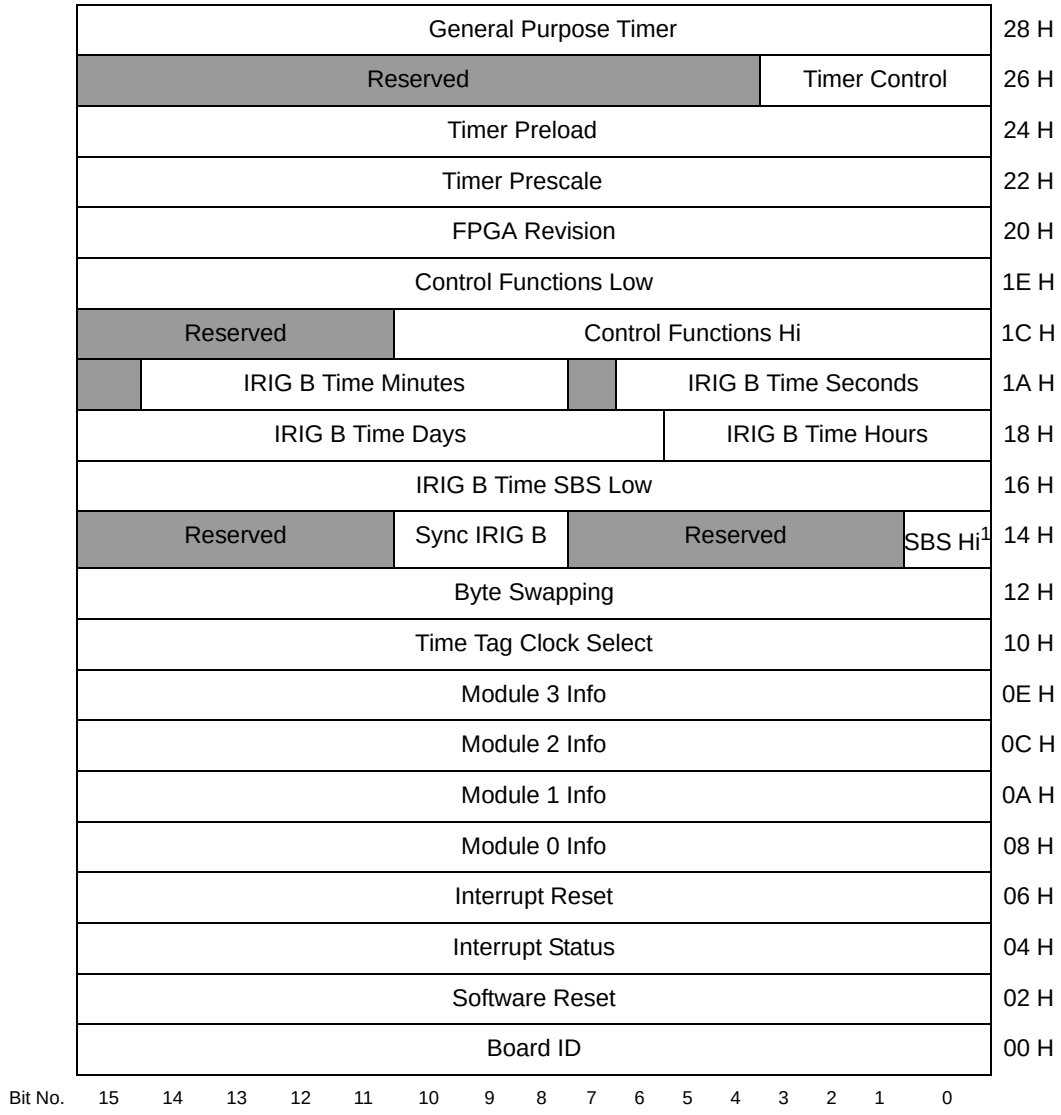

Figure 2-3 *EXC-4000PCI[e]* Global and IRIG B Registers Map

1. IRIG B Time SBS Hi Register

2.6.1 Board Identification Register

Address: 00 (H)
Length 16 bits

Read only The Board Identification register comprises the following identification items.

Bit	Description
04-15	Hard coded to the value 4E0 H
00-03	Selected ID See section **3.3.1 Selected ID DIP Switch [SW1]** on page 3-4.

Table 2-7 Board Identification Register

2.6.2 Software Reset Register

Address: 02 (H)
Length 16 bits

Read/Write The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the module's Time Tag counters.

Bit	Description	
05-15	Reserved – set to 0	
04	Global time tag reset	1 = reset all time tag counters 0 = no effect
03	Module 3 reset	1 = reset module 0 = no effect
02	Module 2 reset	1 = reset module 0 = no effect
01	Module 1 reset	1 = reset module 0 = no effect
00	Module 0 reset	1 = reset module 0 = no effect

Table 2-8 Software Reset Register

2.6.3 Interrupt Status Register

Address: 04 (H)
Length 16 bits

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
05-15	Reserved – set to 0
04	1 = indicates that an interrupt was generated by the General Purpose Timer [See section **2.8 Global Timer Registers** on page 2-22]
03	1 = indicates that module 3 is interrupting
02	1 = indicates that module 2 is interrupting
01	1 = indicates that module 1 is interrupting
00	1 = indicates that module 0 is interrupting

Table 2-9 Interrupt Status Register

Note: See also **2.4.7 DMA Interrupt Status Register** on page 2-13.

2.6.4 Interrupt Reset Register

Address: 06 (H)
Length 16 bits

Write only The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
05-15	Reserved – set to 0
04	1 = Resets General Purpose Timer interrupt 0 = No effect
03	1 = Resets module 3 interrupt 0 = No effect
02	1 = Resets module 2 interrupt 0 = No effect
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Table 2-10 Interrupt Reset Register

Note: See also **2.4.7 DMA Interrupt Status Register** on page 2-13.

2.6.5 Module Info Registers

Address: 08, 0A, 0C, 0E (H)
Length 16 bits each

Read only The Module Info Registers provide identification information for each of the modules.

Bit	Description	
12-15	Module ID	00 H = Module 0 Info register 01 H = Module 1 Info register 02 H = Module 2 Info register 03 H = Module 3 Info register
05-11	Reserved – set to 0	
00-04	Module type[1]	02 H = M4KSerial 04 H = M4K429RTx module 05 H = M4K1553Px module 06 H = M4KMMSI module 07 H = M4K708 module 0C H = M4KCAN module 0D H = M4KDiscrete module 1F H = no module installed

Table 2-11 Module Info Registers

1. For Module 0, if installed, the Module type is fixed to a value of 0D H
For Module 1, if installed, the Module type is fixed to a value of 02 H
For Module 2, if installed, the Module type is fixed to a value of 05 H

2.6.6 Time Tag Clock Select Register

Address: 10 (H)
Length 16 bits

Read/Write The Time Tag Clock Select Register is used to set either an internal (1 MHz) or external source for the board's Global Time Tag Clock. See section **3.4.3 Modules 0, 1 and 2 and External Signals Connector [P2]** on page 3-10, for details of the External Time Tag Clock.

Bit	Description	
01-15	Reserved – set to 0	
00	Time Tag Clock Select	1 = External Source 0 = Internal Source [**Default**]

Table 2-12 Time Tag Clock Select Register

2.6.7 Byte Swapping

Address: 12 (H)
Length 16 bits

Read/Write The Byte Swapping Register may be used to swap the high byte with the low byte of the module memory space and the global registers on the *EXC-4000PCI[e]*. This may be useful on some host computers that byte-swap their memory.

Bit	Description	
00-15	A1A1	Enable byte swapping
	Any other value	Disable byte swapping **(Default)**

Table 2-13 Byte Swapping Register

2.6.8 FPGA Revision Register

Address: 20 (H)
Length 16 bits

Read only The FPGA Revision register contains the FPGA revision of the board.

2.7 IRIG B Global Registers

The *EXC-4000PCI[e]* is able to receive and decode standard serial IRIG B time code format signals (1 KHz carrier wave, sine wave - amplitude modulated, 100 peaks per second) via its connector P2. See section **3.4.3 Modules 0, 1 and 2 and External Signals Connector [P2]** on page 3-10.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the modules on the *EXC-4000PCI[e]*.

- 1st Word — Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.
- 2nd Word — Set of bits reserved for decoding various control, identification and other special purpose functions.
- 3rd Word — Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 14 - 1E (H).

See **Figure 2-3 EXC-4000PCI[e] Global and IRIG B Registers Map** on page 2-15 for the location of the registers on the memory map.

Note: The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.

2.7.1 Sync IRIG B Register

Address: 14 (H)
Bits 08 – 10

Read/Write The 3-bit Sync IRIG B register controls the synchronization of a module's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B time registers.

Bit		Description
10	1	Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers
	0	No IRIG B time has been stored in the IRIG B registers. This bit must be reset by the user after the board has written a '1'.
09	1	Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (14-1E [H]) corresponding to the previous valid IRIG B message. If bit 08 is set, then the IRIG B time will be stored at the same time that the Time tags are reset. To calculate the realtime to which the Time tags are synchronized the user will need to **add** '1' to the value of the IRIG B time stored into these registers.
	0	The previous valid IRIG B message should not be stored in the IRIG B registers. This bit will be automatically reset by the board after the storage of the IRIG B time.
08	1	Resets and synchronizes Time Tags of all the modules to the next rising edge of the on-time Reference Point **Pr** of the IRIG B signal. Also sets Bit 09 to a value of '1' in order to store and display the IRIG B time and control functions into the 6 IRIG B registers.
	0	No reset/synchronization of Time tags relative to the **Pr** of the IRIG B signal. This bit will be automatically reset by board after reset of time tags

Table 2-14 Sync IRIGB Register

Note: All bits are read and write.

2.7.2 IRIG B Time SBS High Register

Address: 14 (H)
Bit 0

Read only The IRIG B Time SBS High register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.7.3 IRIG B Time SBS Low Register

Address: 16 (H)
Bits 15 – 0

Read only The IRIG B Time SBS Low register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.7.4 IRIG B Time Days Register

Address: 18 (H)
Bits 15 – 6

Read only The IRIG B Time Days register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

2.7.5 IRIG B Time Hours Register

Address: 18 (H)
Bits 5 – 0

Read only The IRIG B Time Hours register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.

2.7.6 IRIG B Time Minutes Register

Address: 1A (H)
Bits 14 – 8

Read only The IRIG B Time Minutes register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.

2.7.7 IRIG B Time Seconds Register

Address: 1A (H)
Bits 6 – 0

Read only The IRIG B Time Seconds register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.

2.7.8 Control Functions Registers

Hi Register Address: 1C (H) / Bits 10 – 0
Low Register Address: 1E (H) / Bits 15 – 0

Read only The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.

2.7.9 FPGA Revision Register

Address: 20 (H)
Bits 15 – 0

Read only The FPGA Revision register contains the FPGA revision of the board.

2.8 Global Timer Registers

See **Figure 2-3 EXC-4000PCI[e] Global and IRIG B Registers Map** on page 2-15 for location of the registers on the memory map.

2.8.1 Timer Prescale Register

Address: 22 (H)
Bits 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Table 2-15 Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.8.2 Timer Preload Register

Address: 24 (H)
Bits 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.8.3 Timer Control Register

Address: 26 (H)
Bits 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1	Causes global reset of all installed modules
		0	No effect
02	Interrupt on count completed	1	Output an interrupt (see section **2.6.3 Interrupt Status Register** on page 2-17)
		0	No effect
01	Reload mode	1	Reload mode
		0	Non-reload/One-shot mode
00	Start/Stop	1	Start
		0	Stop

Table 2-16 Timer Control Register

2.8.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value

will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-4500ccVPX* board.

3.1 Board Layout

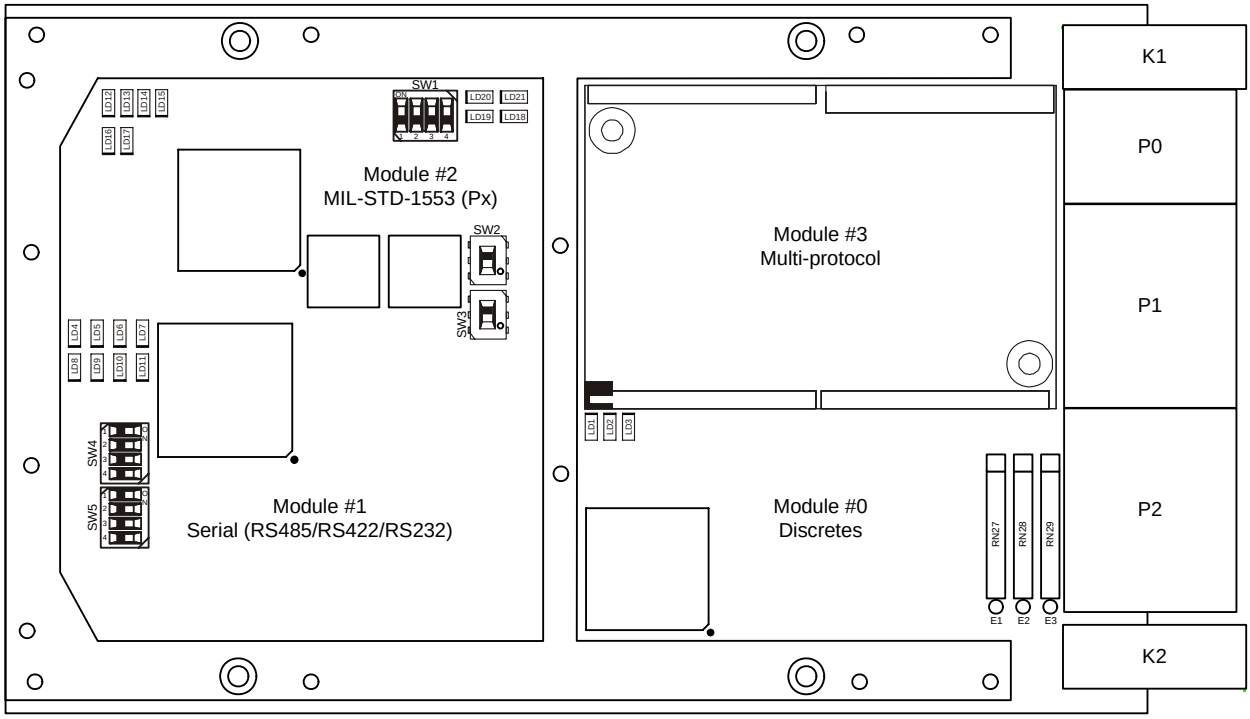

Figure 3-1 *EXC-4500ccVPX* Board Layout

3.2 LED Indicators

The *EXC-4500ccVPX* contains 20 LEDs for the built-in modules and the carrier board. For information on the removable module's LEDs (Module 3), see the module's user's manual.

Location	LED	Color	Indication
Module 0 M4KDiscrete	**LD1**	Green	Module Started
	LD2	Red	Trigger Received on Module
Module 1 M4KSerial	**LD4**	Green	Transmit Active on Channel 0
	LD5	Green	Transmit Active on Channel 1
	LD6	Green	Transmit Active on Channel 2
	LD7	Green	Transmit Active on Channel 3
	LD8	Yellow	Receive Active on Channel 0
	LD9	Yellow	Receive Active on Channel 1
	LD10	Yellow	Receive Active on Channel 2
	LD11	Yellow	Receive Active on Channel 3
Module 2 M4K1553Px	**LD12**	Red	Module Ready
	LD13	Green	BC/Concurrent RT Mode Active[1]
	LD14	Yellow	RT Mode Active[1]
	LD15	Green	Monitor Mode Active
	LD16	Yellow	Bus A Active
	LD17	Green	Bus B Active
Carrier Board	**LD18**	Green	Module 0 Ready
	LD19	Green	Module 1 Ready
	LD20	Green	Module 2 Ready
	LD21	Green	Module 3 Ready

Table 3-1 LED Indicators

1. Not used on single-function modules (*PxS*)

3.3 DIP Switches

The *EXC-4500ccVPX* contains five DIP switches (SW1 – SW5).

3.3.1 Selected ID DIP Switch [SW1]

This four contact DIP switch provides the board's 'Select ID'. (See **3.1 Board Layout** on page 3-2.) It represents a four bit number of which position #1 is the most significant bit. When a specific bit of the switch is:

- **Off** a value of "1" will be set for that bit
- **On** a value of "0" will be set for that bit

Multiple Board Applications

To provide a unique 'Selected ID', to identify a board by the application software in a multiple board application, the DIP switch should be set differently for each board. For example:

Board	ID#1	ID#3
Bit 1	On	On
Bit 2	On	On
Bit 3	On	Off
Bit 4	Off	Off

Table 3-2 Dip Switch settings for unique 'Selected ID'

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the 'unique ID' to match that set on the DIP switch shown in Figure 3-2.

Select ID	Bit 1	Bit 2	Bit 3	Bit 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1

Table 3-3 Selected ID Bits

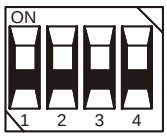

Figure 3-2 DIP Switch SW1 with All Switches Set to ON (Select ID#0)

3.3.2 1553 Coupling Mode Select DIP Switches [SW2, SW3]

Module 3 can be either direct-coupled or transformer-coupled to the 1553 bus. DIP switches are used to select the coupling mode for each bus. (See **3.1 Board Layout** on page 3-2.)

Table 3-4 defines the DIP switch settings for selecting the coupling mode:

Coupling Mode	Switch Position
Direct-Coupled	At the white marker
Transformer-Coupled	Away from the white marker

Table 3-4 DIP Switch Settings Required to Select Coupling Mode

Table 3-5 defines the DIP switch for each Bus:

Bus	DIP Switch
A	SW3
B	SW2

Table 3-5 Bus DIP Switch

Example: To set Bus B to direct-coupled mode, set switch SW2 to the white marker.

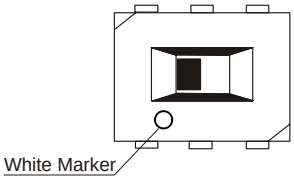

Figure 3-3 DIP Switch – Top View

Factory Default DIP Switch Settings

The factory default settings are:

DIP Switch	Switch Position	Coupling Mode
SW3 (Bus A)	Away from the white marker	Transformer Coupled
SW2 (Bus B)	Away from the white marker	Transformer Coupled

Table 3-6 Factory Default DIP Switch Settings

3.3.3 Serial Configuration DIP Switches [SW4, SW5]

Module 1 has two DIP switches, SW4 and SW5. (See **3.1 Board Layout** on page 3-2.) The DIP switches set the serial communication for each channel:

- SW4 – either half duplex (RS-485) or full duplex (RS-422)
- SW5 – either RS-232 or RS-485 (half and full duplexes)

The number of the DIP switch segment conforms to the channel number.

The module powers up with the serial communication type selected through the DIP switches. After power-up, the communication type can be modified via the DIP switches, or via the register if this feature is enabled. For more information, see **Channel Control Registers** and **Enable Software Selection of Communication Type Register** in the *M4KSerial Module User's Manual*.

Serial Communication	Channel Number	SW4 Segment #				SW5 Segment #			
		1	2	3	4	1	2	3	4
RS-232	0	ON				ON			
	1		ON				ON		
	2			ON				ON	
	3				ON				ON
RS-485 Half Duplex	0	OFF				OFF			
	1		OFF				OFF		
	2			OFF				OFF	
	3				OFF				OFF
RS-422 Full Duplex	0	ON				OFF			
	1		ON				OFF		
	2			ON				OFF	
	3				ON				OFF

Table 3-7 Channel Configuration DIP Switches

Factory DIP Switch Settings

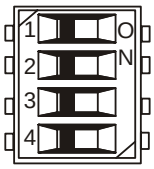

Figure 3-4 DIP Switch – Top View

The factory default settings are:

DIP Switch	Switch Position	Serial Communication
SW4	All segments to ON	RS-232
SW5	All segments to ON	

Table 3-8 Factory Default DIP Switch Settings

3.4 Connectors

The *EXC-4500ccVPX* contains the following connectors:

1. A 56-pin VPX power connector [P0]. The connector pinouts and signals are described in Table 3-9 on page 3-8.

P/N: Tyco® 1410189-3	Left End Half Module VPX Plug-in Connector

   The mating connector is:

P/N: Tyco® 1410186-1	Left End Half Module VPX Back Plane (Plug-in Mating) Connector

2. A 112-pin VPX differential connector [P1] for PCI Express and Module 3 signals. The connector pinouts and signals are described in Table 3-11 on page 3-9.

P/N: Tyco® 1410187-3	Center Module VPX Plug-in Differential Connector

   The mating connector is:

P/N: Tyco® 1410140-1	Center Module VPX Back Plane (Plug-in Mating) Connector

3. A 112-pin VPX single-ended connector [P2] for passing signals for modules 0, 1 and 2 and external signals. The connector pinouts and signals are described in Table 3-13 on page 3-10.

P/N: Tyco® 1410190-3	Center Module VPX Plug-in Single-ended Connector

   The mating connector is:

P/N: Tyco® 1410142-1	Right End Module VPX Back Plane (Plug-in Mating) Connector

3.4.1 Power Connector [P0]

A 56-pin (8-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in left end half module VPX connector [P0] (P/N: Tyco® 1410189-3) provides all power required by the *EXC-4500ccVPX* board. It mates with P/N: Tyco® 1410186-1.

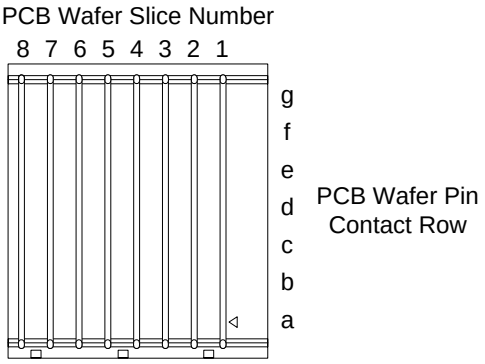

Figure 3-5 Power Connector [P0]

3.4.1.1 Power Connector [P0] Pin Assignments

PCB Wafer Slice Number	PCB Wafer Pin Contact Row						
	Row G	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	+12V	+12V	+12V	N/C	RESERVED	RESERVED	RESERVED
2	+12V	+12V	+12V	N/C	RESERVED	RESERVED	RESERVED
3	+5V	+5V	+5V	N/C	+5V	+5V	+5V
4	RESERVED	RESERVED	GND	RESERVED	GND	SYSRESETn	RESERVED
5	RESERVED	RESERVED	GND	RESERVED	GND	RESERVED	RESERVED
6	RESERVED	RESERVED	GND	RESERVED	GND	RESERVED	RESERVED
7	RESERVED	GND	RES.	RESERVED	GND	RESERVED	RESERVED
8	GND	RESERVED	RESERVED	GND	PCIe_REF_CLK-	PCIe_REF_CLK+	GND

Table 3-9 Power Connector [P0] Pin Assignments

Note: The suffix 'n' represents an active low signal.

Signal Name	Description
SYSRESETn	Global Reset signal (in)
+12V	+12V Power Supply (in)
+5V	+5V Power Supply (in)
GND	Ground
PCIe_REF_CLK-/+	PCI Express 100MHz differential clock (in)
RESERVED	Reserved – Do not connect any signals to this pin
N/C	Pin not connected

Table 3-10 Power Connector [P0] Signal Descriptions

3.4.2 PCI Express and Module 3 Connector [P1]

A 112-pin (16-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in center module differential connector [P1] (P/N: Tyco® 1410187-3) provides all the required PCI Express and Module 3 I/O signals. It mates with P/N: Tyco® 1410140-1.

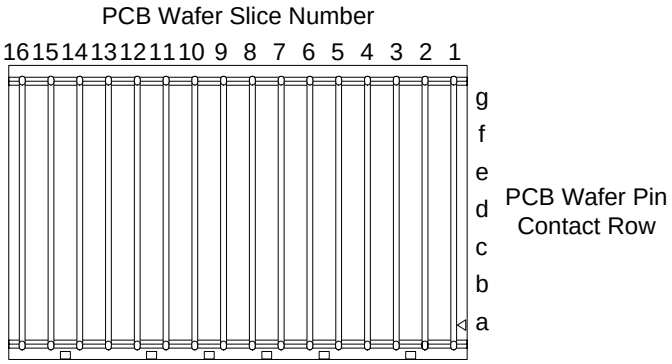

Figure 3-6 PCI Express and Module 3 Connector [P1]

3.4.2.1 PCI Express and Module 3 Connector [P1] Pin Assignments

PCB Wafer Slice Number	PCB Wafer Pin Contact Row						
	Row G	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	RESERVED	GND	TXn	TX	GND	RXn	RX
2	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND
3	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
4	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND
5	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
6	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND
7	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
8	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND
9	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
10	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND
11	RESERVED	GND	M3:TS21	M3:TS22	GND	M3:TS23	M3:TS24
12	GND	M3:TS17	M3:TS18	GND	M3:TS19	M3:TS20	GND
13	RESERVED	GND	M3:TS13	M3:TS14	GND	M3:TS15	M3:TS16
14	GND	M3:TS10	M3:TS11	GND	M3:TS1	M3:TS12	GND
15	RESERVED	GND	M3:TS6	M3:TS7	GND	M3:TS8	M3:TS9
16	GND	M3:TS2	M3:TS3	GND	M3:TS4	M3:TS5	GND

Table 3-11 PCI Express and Module 3 Connector [P1] Pin Assignments

Note: The suffix 'n' represents an active low signal.

Signal Name	Description
TXn	PCI Express x1 lane **transmit** output differential **negative** signal (output)
TX	PCI Express x1 lane **transmit** Output differential **positive** signal (output)
RXn	PCI Express x1 lane **receive** Input differential pair **negative** signal (input)
RX	PCI Express x1 lane **receive** Input differential pair **positive** signal (input)
GND	Ground
M3:TS1 – M3:TS24	I/O signals for removable Module 3 (See Module Terminal Stick pin assignments for the specific removable module.)
RESERVED	Reserved – Do not connect any signals to this pin

Table 3-12 PCI Express and Module 3 Connector [P1] Signal Descriptions

3.4.3 Modules 0, 1 and 2 and External Signals Connector [P2]

A 112-pin (16-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in center module single-ended connector [P2] (P/N: Tyco® 1410190-3) provides all the I/O signals for modules 0, 1 and 2, as well as the external signals. It mates with P/N: Tyco® 1410142-1.

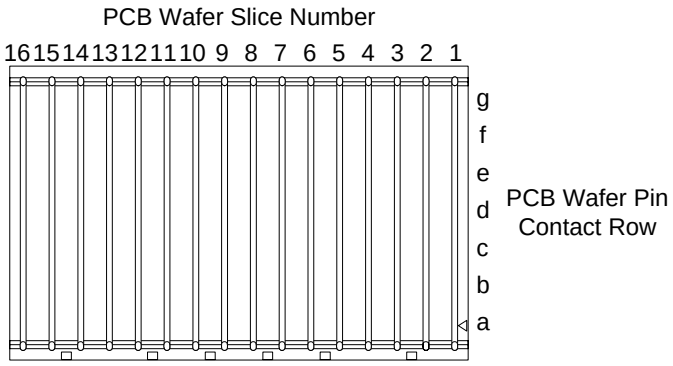

Figure 3-7 Modules 0, 1 and 2 and External Signals Connector [P2]

3.4.3.1 Modules 0, 1 and 2 and External Signals Connector [P2] Pin Assignments

PCB Wafer Slice Number	PCB Wafer Pin Contact Row						
	Row G	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	EXTTCLKI	EXTTRSTn	GND	IRIGB	GND	EXTTCLKO	EXTTRSOn
2	RTLOCKn	GND	GND	RESERVED	GND	RESERVED	EXTTRIGn
3	RTA2	RTA3	GND	GND	GND	RTA4	RTPTY
4	BUSBLO	BUSBHI	GND	EXSTARTn	GND	RTA0	RTA1
5	RESERVED	RESERVED	GND	SHIELD	GND	RESERVED	RESERVED
6	BUSALO	BUSAHI	GND	SHIELD	GND	RESERVED	RESERVED
7	485_422T3	232T_485n_422Tn3	GND	RESERVED	GND	232R_422R3	422Rn3
8	232R_422R2	422Rn2	GND	SHIELD	GND	GND	RESERVED
9	232R_422R1	422Rn1	GND	RESERVED	GND	485_422T2	232T_485n_422Tn2
10	GND	RESERVED	GND	SHIELD	GND	485_422T1	232T_485n_422Tn1
11	485_422T0	232T_485n_422Tn0	GND	RESERVED	GND	232R_422R0	422Rn0
12	IO15	IO16	GND	RESERVED	GND	GND	IO17
13	IO11	IO12	GND	IO19	GND	IO13	IO14
14	IO8	EXT_TRIGn	GND	IO18	GND	IO9	IO10
15	IO5	IO6	GND	SHIELD	GND	GND	IO7
16	IO1	IO2	GND	IO0	GND	IO3	IO4

Table 3-13 Modules 0, 1 and 2 and External Signals Connector [P2] Pin Assignments

Note: The suffix 'n' represents an active low signal.

Signal Name	Description		
Module 0: Discrete I\O			
IO0 – IO19	Discrete 0 – Discrete 19		
EXT_TRIGn	TTL Active low external trigger (pulse width approx. 150 nS)		
Module 1: Serial – 2 Channels (X=0,1); Serial – 4 Channels (X=0,1,2,3)			
	RS-232	**RS-485**	**RS-422**
485/422Tx	N/C	Channel x high line connection	Channel x transmit high line connection
232T/485n/422Tnx	Channel x transmit line connection	Channel x low line connection	Channel x transmit low line connection
232R/422Rx	Channel x receive line connection	N/C	Channel x receive high line connection
422Rnx	N/C	N/C	Channel x receive low line connection
Module 2: 1553			
BUSALO	Bus A connection low		
BUSAHI	Bus A connection high		
BUSBLO	Bus B connection low		
BUSBHI	Bus B connection high		
RTA0	Single function module (*PxS*) RT address bit position 0 input		
RTA1	Single function module (*PxS*) RT address bit position 1 input		
RTA2	Single function module (*PxS*) RT address bit position 2 input		
RTA3	Single function module (*PxS*) RT address bit position 3 input		
RTA4	Single function module (*PxS*) RT address bit position 4 input		
RTPTY	Single function module (*PxS*) RT address parity bit input		
RTLOCKn	Single function module (*PxS*) RT address lock		
EXSTARTn	External Start		
Board Level Specific Signals			
SHIELD	Provides the input and output channels with shield connections.		
GND	Provides ground reference for input and output channels.		
EXTTCLKI	External Time Tag Clock Input (Nominal value: 1MHz). This signal supplies an external global clock for the Time Tags of all the modules. Use this signal to synchronize the Time Tags that are implemented on the modules to other boards or systems.		
EXTTCLKO	Global Time Tag Clock TTL Output (1 MHz). This signal is the Global Clock that is supplied to all the modules for their Time Tags. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. The source of this clock is either the External Time Tag Clock EXTTCLKI or the Internal Time Tag Clock.		
EXTTRSTn	External Time Tag reset TTL Input. Use this low active pulsed signal (minimum 100 nsec.wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems.		
EXTTRSOn	Global Time Tag Reset TTL Output**.** This low active signal is activated each time a Global Time Tag Reset is applied. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. This signal is activated by either the internal Global Time Tag signal or from the External Time Tag signal (EXTTRSOn).		
IRIG B	IRIG B Input**.** This should be a 1KHz sine wave, amplitude modulated, IRIG B signal with a 3:1 modulation ratio at 3V typical.		

Table 3-14 Modules 0, 1 and 2 and External Signals Connector [P2] Signal Descriptions

3.4.3.2 Synchronizing with an External Source

To synchronize a single *EXC-4500ccVPX* board to an external system, the external clock source and the external reset must be connected to the EXTTCLKI and the EXTTRSTn signals respectively.

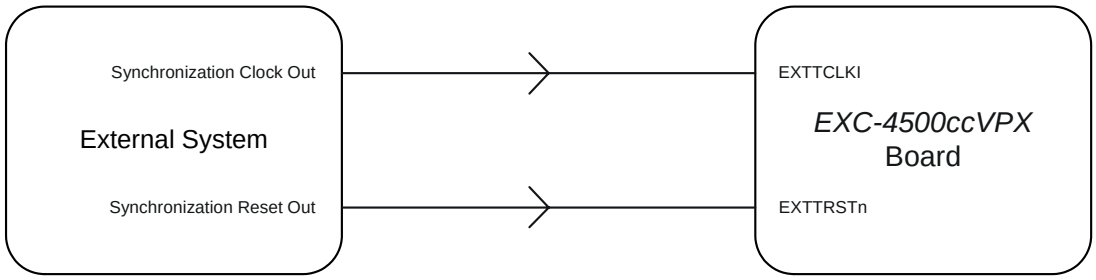

Figure 3-8 Synchronization of a Single *EXC-4500ccVPX* Board to an External System

To synchronize an external system to a single *EXC-4500ccVPX* board, the EXTTCLKO and the EXTTRSOn signals need to be connected to the external clock source and the external reset respectively.

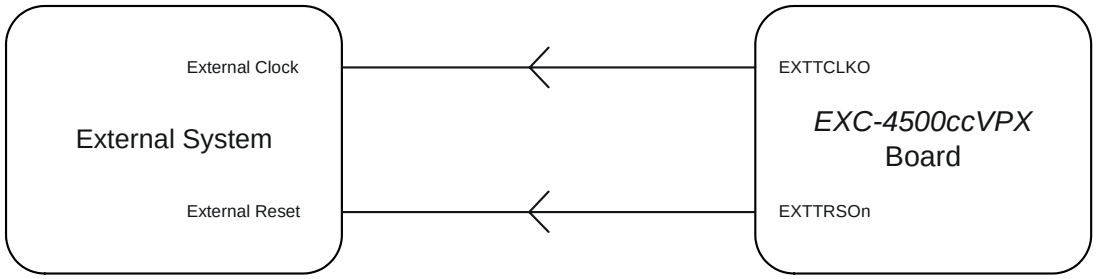

Figure 3-9 Synchronization of an External System to a Single *EXC-4500ccVPX* Board

Warning: The synchronization clock and reset signals may be connected to multiple targets to achieve system wide synchronization.

3.4.3.3 Synchronizing Between *EXC-4500ccVPX* Boards

To synchronize multiple *EXC-4500ccVPX* boards the **EXTCLKO** and the **EXTTRSOn** signals of one board need to be connected to all the **ETTCLKI** and the **EXTTRSTn** signals respectively, of the remaining boards.

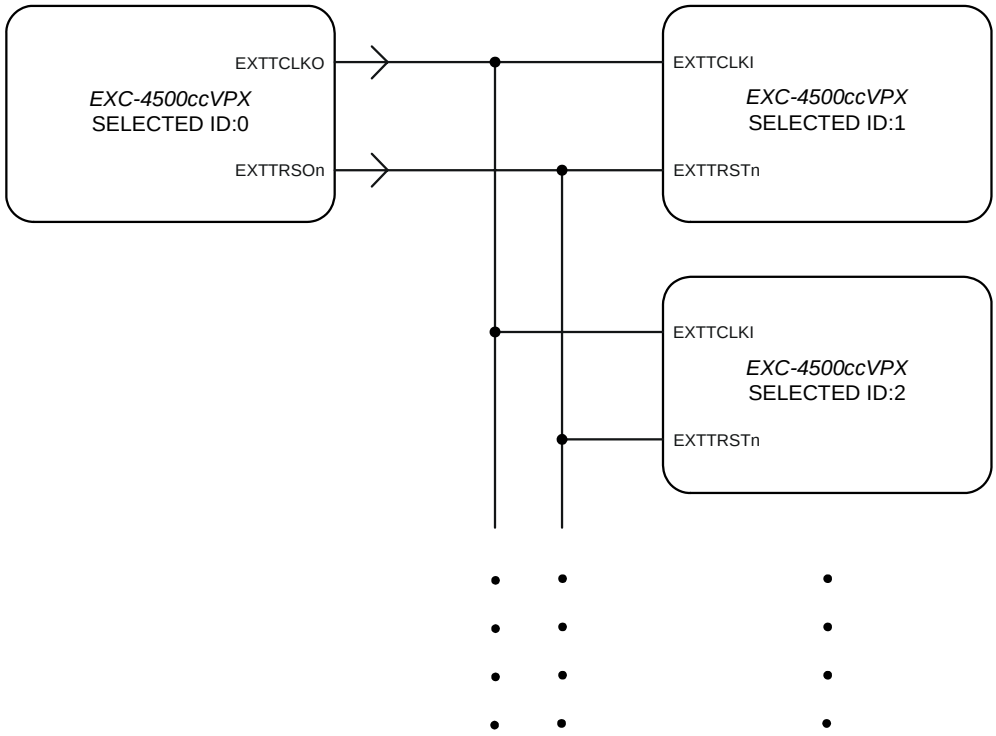

Figure 3-10 Synchronization Between *EXC-4500ccVPX* Boards

3.5 Power Requirements

The *EXC-4500ccVPX* standby power requirements, with the three onboard modules, are:

+5V	+12V
1.8A	20mA

The total operating power requirements depend on which modules are running. See the user's manual for each module for further information.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering an *EXC-4500ccVPX* carrier board.

Part Number	Option	Description
EXC-4500ccVPX/M$_0$M$_1$M$_2$M$_3$		Multi-protocol interface board for VPX compatible systems.
	-E	Extended temperature option (-40° to +85°C).
	-001	With conformal coating.

Note: Replace ***M$_0$***, ***M$_1$***, ***M$_2$***, and ***M$_3$*** with the module codes (specified in the following table) to specify the modules that you want to order with the *EXC-4500ccVPX*.

Module 0 must be an M4KDiscrete (ordering code **I*x***).

Module 1 must be an M4KSerial2 (ordering code **J*x***) or M4KSerial4 (ordering code **K*x***).

Module 2 must be an M4K1553Px (ordering code **F*x***), M4K1553PxS (ordering code **T*x***), M4K1553PxM (ordering code **V*x***), M4K1553Px-1760 (ordering code **L*x***) or M4K1553PxS-1760 (ordering code **U*x***).

Module 3 can be any of the types listed below.

Module Code (for Ordering with *EXC-4500ccVPX*)	Module Part # (for Ordering Separately)	Option	Description
A*x*	**M4K429RT5**		ARINC 429 interface module: supports up to five channels.
B*x*	**M4K429RT10**		ARINC 429 interface module: supports up to ten channels.
C*x*	**M4K708**		The module supports two ARINC 708/ 453 channels, each one selectable as either transmit or receive.
F*x* (or G*x*)	**M4K1553Px**		MIL-STD-1553 interface module: supports BC, multiple RTs, BC/ Concurrent-RT and Bus Monitor modes. Supports an Internal Concurrent Monitor in RT and BC/RT modes.
H*x*	**M4K1553PxS-1760**		Single-function MIL-STD-1760 interface module: supports single RT, BC, and Bus Monitor modes with an Internal Concurrent Monitor in RT and BC modes. Without error injection.
I*x*	**M4KDiscrete**		Discrete interface module: supports 20 bi-directional discretes with TTL (0 – 5V) or Avionic (0 – 32V) levels.
J*x*	**M4KSerial2**		Serial Interface module: supports two independent channels with RS485, RS422 or RS232 communication.

Table 4-1 M4K Module Codes and Part Numbers

Module Code (for Ordering with *EXC-4500ccVPX*)	Module Part # (for Ordering Separately)	Option	Description
K*x*	M4KSerial4		Same as above - supports four independent channels.
L*x* (or M*x*)	M4K1553Px-1760		MIL-STD-1553 interface module: supports BC, multiple RTs, BC/ Concurrent-RT and BM modes with MIL-STD-1760 option. Supports an Internal Concurrent Monitor in RT and BC/RT modes.
O*x*	M4KCAN2		2 independent channels of CAN 2.0 B protocol with standard and extended message frames and message identifiers.
P*x*	M4KCAN4		Same as above with 4 independent channels.
Q*x*	M4KCAN6		Same as above with 6 independent channels.
R*x*	M4KMMSI		Mini Munitions Store Interface (MMSI) module. Supports RT, BC/Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 8 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and 1 composite monitor output.
T*x*	M4K1553PxS		Single-function MIL-STD-1553 interface module: supports single RT, BC, and Bus Monitor modes with an Internal Concurrent Monitor in RT and BC modes. Without error injection.
V*x*	M4K1553PxM		Monitor-only MIL-STD-1553 interface module.
		-E	Add this suffix for an extended temperature/ruggedized version of any module. The ruggedized version has an extended temperature range of -40º to +85º C.
		-001	Add this suffix for conformal coating.

Table 4-1 M4K Module Codes and Part Numbers (Continued)

More modules are in design. Check our website for the latest modules: www.mil-1553.com.

Note:

1. Use the **Module Part #** when ordering separately from the *EXC-4500ccVPX*.
2. Use the **Module Codes** when ordering modules with the *EXC-4500ccVPX*.
3. When ordering a board with a number of different protocol modules, the part number of the board must be in the following form:

   EXC-4500ccVPX/I1J1F1C1

   The first module code in the part number is Module 0, the second is Module 1, and so on.

4. If one or more empty module locations are required, insert an asterisk (*) followed by the number of empty locations, for example, *2.

Example: EXC-4500ccVPX/I1K1F1O1

This is an *EXC-4500ccVPX* carrier board with:
1 M4KDiscrete module at module locations 0
1 M4KSerial4 module at module location 1
1 M4K1553Px modules at module location 2
1 M4KCAN2 modules at module location 3

Example: EXC-4500ccVPX/I1*1F2

This is an *EXC-4500ccVPX* carrier board with:
1 M4KDiscrete module at module location 0
Empty slot at module location 1
1 M4K1553Px module at module location 2
1 M4K1553Px modules at module location 3

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